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Course Code 

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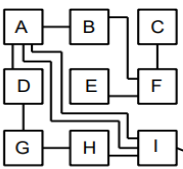
Seventh Semester B.E. Degree Examinations, February 2025

**ADVANCED VLSI DESIGN AND TESTING**

Duration: 3 hrs

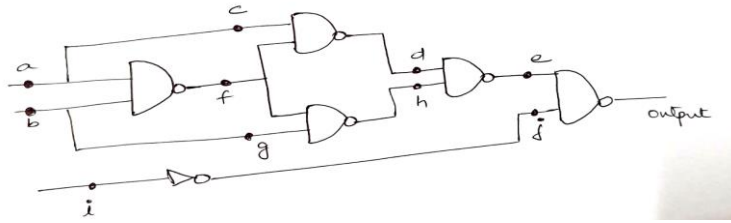
Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.  
2. Missing data, if any, may be suitably assumed

<u>Q. No</u>	<u>Question</u>	<u>Marks</u>	<u>(RBTL:CO:PI)</u>
<b><u>Module-1</u></b>			
1.	a. Explain the semi-custom ASIC design flow with example for each step.	08	(2:1:2.1.1)
	b. Design a 6-bit Ripple Carry Adder and show the outputs for cases when carry-in is 0 and when carry-in is 1. Write truth table for $2^n$ inputs with $n=3$ .	08	(3:1:2.1.1)
	c. Write a short note on standard cell libraries.	04	(2:1:1.1.1)
(OR)			
2.	a. Design an 8-bit Carry Bypass Adder and show outputs for varying the control lines of Mux. Generate the truth table for varying inputs and carry outputs.	10	(3:1:2.1.1)
	b. Define ASIC design. Explain the importance of ASIC's by considering various issues in the VLSI circuits.	10	(3:1:2.1.1)
<b><u>Module-2</u></b>			
3.	a. With the help of fixed blocks, mention the various tools used in the Floor planning of cell-based ASIC design.	06	(2:2:3.1.1)
	b. Show how the capacitance value is decreased drastically with the help of flow diagram in the physical design flow.	06	(3:2:3.1.1)
	c. Explain various iterative placement methods with example for each method.	08	(2:2:3.1.1)
(OR)			
4.	a. Explain the path formed between node A and node I.	06	(2:2:3.1.1)
			
	Explain with the help of iterations.		
	b. Define Fanout? Explain its importance with respect to delay calculation.	06	(3:2:3.1.1)
	c. Given three blocks with the following potential widths and heights. Generate the bounding box and calculate total area with the help of aspect ratio.	08	(2:2:3.1.1)
	Block A: $w=1, h=4$ (or) $w=4, h=1$ (or) $w=2, h=2$		
	Block B: $w=1, h=2$ (or) $w=2, h=1$		
	Block C: $w=1, h=3$ (or) $w=3, h=1$		

### Module-3

5. a. The circuit shown in Q5 (a) has 10 fault sites and 20 single stuck at faults. Generate the fault matrix and identify the faulty paths. 10 (3:3:4.1.3)



Q5 (a)

- b. Demonstrate the path delay and transition delay fault methods. 10 (3:3:4.1.3)
- (OR)
6. a. Explain the path sensitization technique with the help of netlist for the Boolean equation  $Y=AB+C$ . Also generate the 'n' test vectors to identify the faulty path. 06 (3:3:4.1.3)
- b. Design a two input CMOS NAND Gate and identify the stuck-open and stuck-short faults. Mention test vectors in the truth table. 08 (3:3:4.1.3)
- c. Illustrate the importance of the clock period in identifying the faults and with the help of netlist explain the distributed and lumped faults. 06 (3:3:4.1.3)

### Module-4

7. a. Write a short note on sequential circuit testing and also design a 6-bit serial adder. 10 (3:4:4.2.1)
- b. Explain the test vector generation using the Boolean difference method for the given function  $F=(A+B)C'+CD$  06 (3:4:4.2.1)
- c. Write the importance of the Boolean difference method to generate the test vectors. 04 (2:4:4.2.1)

(OR)

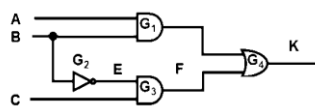
8. a. Create the test generation for the function  $Y=(A+B)+CD+E'$  using netlist and truth table by mentioning the advantages of each method. 10 (3:4:4.2.1)
- b. How do the ad-hoc strategies differ from the structured scan-based methods for testing manufactured circuits, and which approach, when justified with an example, proves to be the more effective choice? 10 (3:4:4.2.1)

### Module-5

9. a. Design the complete feedback shift register with the help of signature analyzer. 10 (3:5:4.2.2)
- b. With the help of block diagram, elaborate the methodology of implementing BIST and the approach of generating BIST patterns. 10 (3:5:4.2.2)

(OR)

- 10 a. Provide a concise explanation of BIST and design a shift register employing linear feedback for the polynomial  $f(x) = 1+x+x^3$  10 (3:5:4.2.2)
- b. Explain the BIST Hierarchy with a neat block diagram? Also, for the netlist given Q 10 (b) identify the following : 10 (3:5:4.2.2)
- (i) Number of path delay faults
- (ii) Does  $ABC = 001 \rightarrow 011$  detect  $\uparrow$ BEFK



Q 10 (b)

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