

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

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Course Code

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Third Semester B.E. Degree Examinations, January 2025

DIGITAL ELECTRONICS

Duration: 3 hrs

Max. Marks: 100

Note: 1. Answer any FIVE full questions choosing ONE full Question from each Module.
 2. Missing data, if any, may be suitably assumed

<u>Q. No</u>	<u>Question</u>	<u>Marks</u>	<u>(RBTL:CO:PI)</u>
<u>Module-1</u>			
1.	a. Explain the design steps in combinational logic with neat diagram.	10	(2 :1: 1.3.1)
	b. Determine all PI and EPI for the following functions using Quine-McCluskey method $f(a, b, c, d) = \sum m(1, 3, 4, 5, 7, 8, 11, 12, 15)$	10	(3 :1: 2.1.2)
(OR)			
2.	a. Distinguish between combinational and sequential circuits with block diagram and examples for each.	10	(2 :1: 1.3.1)
	b. Determine the POS expression for the following Boolean function using K-map. $f(a, b, c, d) = \prod M(0, 1, 4, 8, 10, 11, 12, 16, 17, 20, 22, 24, 25, 26)$	10	(3 :1: 2.1.2)
<u>Module-2</u>			
3.	a. Write a note on decoders and encoders with neat block diagrams and examples.	10	(2 :2: 1.3.1)
	b. Explain the process of cascading the decoders using IC74138 and implement the following Boolean functions using IC74138 $F1 = f(w, x, y, z) = \sum (1, 2, 4, 6, 9) \quad F2 = f(w, x, y, z) = \prod M(0, 3, 5, 9, 12, 13)$	10	(3 :2: 2.1.2)
(OR)			
4.	a. Write a note on multiplexers and demultiplexers with neat block diagrams and applications.	10	(2 :2: 1.3.1)
	b. Design 2-bit comparator, with A1, A0 and B1, B0 inputs, represent, truth table, switching equations, k-maps, and logic diagram using basic gates.	10	(3 :2: 2.1.2)
<u>Module-3</u>			
5.	a. Explain the operation of SR latch also application of SR flip-flop as switch debouncer.	10	(2 :3: 1.3.1)
	b. Explain master-slave JK flip flop with logic diagram, symbol, truth table and timing diagram.	10	(2 :3: 1.3.1)
(OR)			

6. a. Explain the process of representing characteristics equations with next state table and k-maps for the following: **10** (2 :3: 1.3.1)
 (i) SR flip flop (ii) JK flip flop
 (iii) T flip flop (iv) D flip flop.
- b. Explain the operation of positive edge triggered D flip flop, with symbol, logic diagram and truth table. **10** (2 :3: 1.3.1)

Module-4

7. a. Explain the following shift register operations with neat diagrams **10** (2 :4: 1.3.1)
 (i) SISO (ii) SIPO (iii) PISO (iv) PIPO
- b. What are ripple counters? Explain the operation of 4-bit binary ripple UP counter, represent neat circuit and waveform. **10** (2 :4: 1.3.1)

(OR)

8. a. Explain the operations of the following with neat diagrams, truth table and waveforms: **10** (2 :4: 1.3.1)
 (i) Ring Counter (ii) Twisted Ring Counter
- b. What is the difference between synchronous and asynchronous counters? **10** (2 :4: 1.3.1)
 Explain the operation of 4-bit synchronous binary counter with neat diagram.

Module-5

9. a. Explain the following: **10** (2 :5: 1.3.1)
 (i) Input and Output variables (ii) State variables
 (iii) Excitation variables (iv) Present State (v) Next State
- b. Construct state table and state diagram for the following sequential circuit shown in Fig. Q9 (b). **10** (3 :5: 2.1.2)

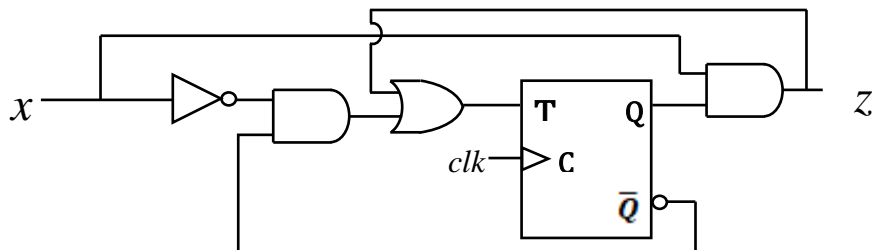


Fig. Q9 (b)

(OR)

10. a. What is state diagram? Explain the construction of State diagram for Moore model and Mealy models with examples. **10** (2 :5: 1.3.1)
- b. Construct state table and state diagram for the following sequential circuit shown in Fig. Q10 (b). **10** (3 :5: 2.1.2)

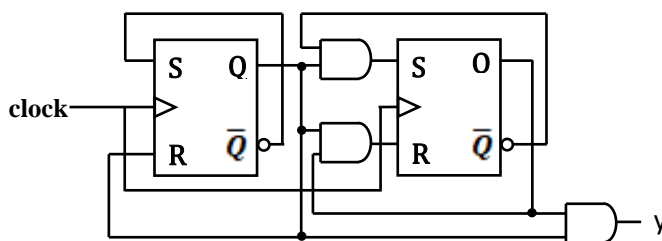


Fig. Q10 (b)

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