2022 SCHEME

Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN										

Course Code 22CS/AI/CA/CD/32

Third Semester B.E. Degree Examinations, January 2025

DIGITAL SYSTEM DESIGN AND COMPUTER ORGANIZATION

(Common to CSE, AIML, CSE- AI, CSE- DS)

Duration: 3 hrs **Max. Marks: 100**

Note: ***1. Answer any* FIVE *full questions choosing ONE full Question from each Module.***
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO:PI)*
		Module-1		
1.	**a.**	Find the minimum SOP and POS expression. Underline the essential prime implicants in your answer and tell which minterm makes each one essential. F(a,b,c,d) = ∏M (5,7, 13, 14,15) • ∏ D (l, 2, 3, 9)	**08**	**(3 :1: 1.7.1)**
	b.	A switching circuit has two control inputs (C1 and C2), Two data inputs (X1 and X2), and one output (Z). The circuit performs one of the logic operations on the two data inputs. The function performed depends on the control inputs.	**06**	**(3 :1: 1.7.1)**

C1	C2	Function performed by circuit
0	0	OR
0	1	XOR
1	0	AND
1	1	EQU

(i) Derive a truth table for Z

(ii) Use a Karnaugh map to find a minimum AND-OR gate circuit to realize Z.

	c.	Given F **= AB'D' + A' B + A'C+ CD**. Use a Karnaugh map to find the minimum SOP of F' and POS of F	**06**	**(3 :1: 1.7.1)**
		(OR)		
2.	**a.**	Identify all essential prime implicants using QMC & prime implicants chart F (a, b, c, d) = ∑m (0,1,3,5,6,7,8,10,14,15).	**10**	**(3 :1: 1.7.1)**
	b.	Solve Using Map Entered Variable Use four Variable Map to Find Minimum SOP Z(a,b,c,d,e,f,g)=∑m(0,3,13,15)+∑d(1,2,7,9,14)+ E(m6+m8)+Fm12+Gm5.	**10**	**(3 :1: 1.7.1)**
		Module-2		
3.	**a.**	Realize the function f(a, b, c, d, e)=∑m(6, 7, 9, 11, 12, 13, 16, 17, 18, 20, 21, 23, 25, 28) using a 16-to-1 MUX, control inputs are **b, c, d, e** , and data inputs should be **a, a',1 or 0**	**08**	**(3 :2: 1.7.1)**
	b.	Build a full adder using a 3-to-8-line decoder and (i) Two OR gates. (ii) Two NOR gates.	**06**	**(3 :2: 1.7.1)**

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)

	c.	Construct Full Subtractor Using PAL	**06**	**(3 :2: 1.7.1)**

(OR)

4.	**a.**	Derive characteristic equations and excitation table for D-FF, T-FF, JK-FF, SR-FF.	**10**	**(3 :2: 1.7.1)**
	b.	Realize the J-K master-slave flip-flop using table and timing diagram.	**10**	**(3 :2: 1.7.1)**

Module-3

5.	**a.**	Explain 4-bit parallel-in, parallel-out shift register	**08**	**(3 :3: 1.7.1)**
	b.	Describe data Transfer between registers with example	**06**	**(3 :3: 1.7.1)**
	c.	Discuss n-Bit parallel adder with Accumulator	**06**	**(3 :3: 1.7.1)**

(OR)

6.	**a.**	Design mod-8 counter which counts in sequence using JK-FF.	**10**	**(3 :3: 1.7.1)**
	b.	Design 3-bit counter which counts in sequence 1→ 4→ 5 → 7 → 6→ 2→ 3→1 using T-FF and D-FF.	**10**	**(3 :3: 1.7.1)**

Module-4

7.	**a.**	Explain connection between memory and processor with neat diagram and example.	**08**	**(2 :4: 1.7.1)**
	b.	Explain basic performance equation and overall SPEC rating of computer.	**06**	**(2 :4: 1.7.1)**
	c.	Explain two ways in which byte addresses are arranged with example.	**06**	**(2 :4: 1.7.1)**

(OR)

8.	**a.**	Explain any 5 addressing modes with examples.	**10**	**(2 :4: 1.7.1)**
	b.	Explain four basic types of instruction and solve Y= (A+B) *(C-D).	**10**	**(2 :4: 1.7.1)**

Module-5

9.	**a.**	Explain handling multiple devices using vectored interrupt and interrupt nesting.	**08**	**(2 :5: 1.7.1)**
	b.	What is DMA? What are it advantages? With supporting diagram, explain different registers used in DMA interface.	**06**	**(2 :5: 1.7.1)**
	c.	What is bus arbitration? Explain types of bus arbitration with neat diagram.	**06**	**(2 :5: 1.7.1)**

(OR)

10	**a.**	Design 16-bit Carry Look Ahead adder using 4-bit adder and compare its performance with Ripple Bit Carry adder.	**10**	**(3 :5: 1.7.1)**
	b.	Apply booth algorithm to perform the multiplication on +13 and -06.	**10**	**(3 :5: 1.7.1)**

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Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)