

Basavarajeswari Group of Institutions
BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT
 (Autonomous Institute under Visvesvaraya Technological University, Belagavi)

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Course Code

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Third Semester B.E. Degree Examinations, September 2024
COMPUTER ORGANIZATION AND ARCHITECTURE

Duration: 3 hrs

Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
 2. Missing data, if any, may be suitably assumed

<u>Q. No</u>	<u>Question</u>	<u>Marks</u>	<u>(RBTL:CO:PI)</u>
Module-1			
1.	a. What is the role of memory and processor when you store addition result in memory after loading A and B values in processor. Also create memory of 64 MB memory of 8-bit word length and draw memory with word address.	04	(2 : 1 : 1.6.1)
	b. Compare single precision and double precision IEEE formats.	06	(2 : 1 : 1.6.1)
	c. Explain the connection between the processor and memory with the help of appropriate diagram. Also write the steps in executing the instruction. sub R1, R0	10	(2 : 1 : 1.6.1)
(OR)			
2.	a. Convert the following pairs of decimal numbers to 4-bit, signed, 2's-complement binary numbers and add them. State whether or not overflow occurs in each case (i) 5 and 7 (iii) 3 and -7	06	(2 : 1 : 1.7.1)
	b. Define (i) clock cycle (ii) Performance (iii) Multitasking (iv) Cache memory (v) Memory access time (vi) Compiler	06	(2 : 1 : 1.6.1)
	c. Write the importance of branching technique and condition codes.	08	(1 : 1 : 1.6.1)
Module-2			
3.	a. Perform following operations and find the results if R ₀ = 1011_1001_1110_0101, Carry bit = 0 (i) LshiftL #2, R ₀ (ii) AshiftR #2, R ₀ (iii) RotateLC #2, R ₀	06	(2 : 2 : 1.7.1)
	b. What is parameter passing? Explain its types.	06	(1 : 2 : 1.6.1)
	c. Write an ALP to add hexadecimal numbers: 32h & 48h and store in the SUM (400h) . Starting address of the program is 100h , reserve the data area of 200 with starting address NUM1 (208) using appropriate assembler directives.	08	(2 : 2 : 1.7.1)
(OR)			
4.	a. Write an ALP to Add two hexadecimal numbers: 23h & 45h and store the result in register R6 using (i) immediate (ii) Direct addressing modes (make use of memory locations 2002, 2004 if needed). Write EA in each case.	06	(2 : 2 : 1.7.1)
	b. Define and explain subroutine and subroutine nesting.	06	(1 : 2 : 1.6.1)
	c. Stack operation is FIFO. Justify using PUSH and POP Code along with appropriate diagrams.	08	(1 : 2 : 1.6.1)
Module-3			
5.	a. Explain polling and simultaneous request methods of handling multiple devices while using interrupts.	06	(1 : 3 : 1.6.1)
	b. How basic I/O operations are performed using program controlled I/O applying concept of single STATUS register.	06	(2 : 3 : 1.6.1)

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI- Performance Indicator)

- c. Write detailed explanation of DMA. **08** (1 :3 : 1.6.1)
- (OR)**
6. a. Write the importance/role of different components used in **I/O interface for an input device** using appropriate block diagram. **06** (1 :3 : 1.6.1)
- b. **Define** (i) ISR (ii) Interrupt (iii) INTA (iv) Interrupt Latency (v) IR (vi) Privileged instructions. **06** (2 :3 : 1.6.1)
- c. Explain interrupt hardware. How does the system prevent from entering into an infinite-loop because of interrupt? **08** (1 :3 : 1.6.1)

Module-4

7. a. Consider the dynamic memory cell of Fig. Q7(a). Assume that the minimum refresh rate is 72 ms and that leakage current through the transistor is about 0.25 Pico amperes (10^{-12} A). The voltage across the capacitor when it is fully charged is 1.5 V. The cell must be refreshed before this voltage drops below 0.9 V. Estimate the capacitor value. **06** (2 :4 : 1.7.1)

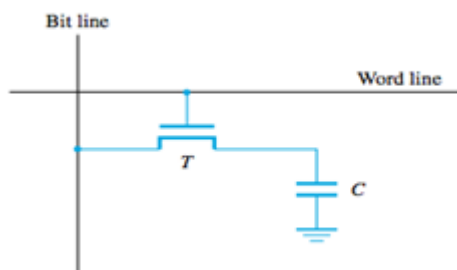


Fig. Q7(a).

- b. Explain **16 × 8** Organization of a memory chip using appropriate diagram **06** (1 :4 : 1.6.1)
- c. Write a short note on virtual memory and ROM. **08** (1 :4 : 1.6.1)
- (OR)**
8. a. A disk unit has 32 recording surfaces. It has a total of 20000 cylinders. There is an average of 600 sectors per track. Each sector contains 512 bytes of data.
(i) What is the maximum number of bytes that can be stored in this unit?
(ii) What is the data transfer rate in bytes/sec at a rotational speed of 7200 RPM? **06** (2 :4 : 1.7.1)
- b. **Define** (i) Cache hit (ii) Cache miss (iii) Read hit (iv) Read miss (v) write hit (vi) write miss **06** (1 :4 : 1.6.1)
- c. Explain floppy disks and RAID disk arrays. **08** (1 :4 : 1.6.1)

Module-5

9. a. Explain single bus organization of the data path inside a processor with the help of appropriate diagram. **06** (1 :5 : 1.6.1)
- b. Show the circuit implementation of Z_{in} generation and end control signal generation using hard wired control. **06** (1 :5 : 1.6.1)
- c. Explain organization of the control unit to allow conditional branching in the micro-program with the help of appropriate diagrams. **08** (1 :5 : 1.6.1)
- (OR)**
- 10 a. Explain a complete processor with the help of appropriate diagram. **06** (1 :5 : 1.6.1)
- b. Explain separate decoding and encoding functions in control unit with the help of appropriate diagram. **06** (1 :5 : 1.6.1)
- c. Write the control sequence for the following instruction using three bus organization along with explanation and appropriate diagram: ADD R4, R5,R6 **08** (1 :5 : 1.6.1)
