

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

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Course Code

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Fourth Semester B.E. Degree Examinations, Sep/Oct 2023

DIGITAL CIRCUITS DESIGN

Duration: 3 hrs

Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. Missing data, if any, may be suitably assumed

Q. No	Question	Marks	(RBTL:CO: PI)
MODULE – 1			
1. a.	Define following terms with examples: i) Minterm and Maxterm ii) Canonical SOP and Canonical POS	04	(1 :1: 1.3.1)
b.	Derive the following expressions in the canonical/standard form: i) $f(w, x, y, z) = (x' + y + z') \cdot (w + x + y') \cdot (w' + y)$ ii) $f(p, q, r, s) = pq + rs + q'r + ps'$	06	(3 :1: 2.1.2)
c.	Determine all the minimal sums and minimal products for the following Boolean function using K-map $f(w, x, y, z) = \sum m(0,2,5,7,8,10,13,15) + \sum d(1,4,11,14)$	10	(3 :1: 2.1.2)
OR			
2. a.	Determine prime implicants for the following incomplete Boolean functions using K-map, indicate which is essential $f(v, w, x, y, z) = \pi M(3,7,8,9,11,12,13,15,16,19,20,23,27,30,31)$	10	(3 :1: 2.1.2)
b.	Determine all PI and EPI for the following functions using Quine-McCluskey method $f(a, b, c, d) = \sum m(0,1,4,5,9,10,12,14,15) + dc(2,8,13)$	10	(3 :1: 2.1.2)
MODULE – 2			
3. a.	Design 4-bit binary to gray code converter combinational logic circuit using 7486IC.	10	(3 :2: 2.1.2)
b.	Implement following multiple output function for both active high outputs and for active low output IC74138 and external gates: $F1=f(w, x, y, z) = \sum m(0,2,5,7,11,13,14)$ $F2=f(w, x, y, z) = \prod M(1,3,4,6,8,10,12,15)$	10	(3 :2: 2.1.2)
OR			
4. a.	Implement the $Z = f(w, x, y, z) = \sum m(0,1,3,4,6,7,9,11,12,14,15)$ function using 4:1 MUX, consider y, z as select inputs.	8	(3 :2: 2.1.2)
b.	Design 4-bit adder with look ahead carry scheme.	6	(3 :2: 2.1.2)
c.	Design 2-bit comparator using logic gates.	6	(3 :2: 2.1.2)
MODULE – 3			
5. a.	Distinguish between sequential circuits and combinational circuits.	6	(2 :3: 1.3.1)
b.	Explain the working of JK Flip-Flop and also represent JK flip flop using NAND-NAND logic diagram.	6	(2 :3: 1.3.1)
c.	Explain master-slave SR flip flop with logic diagram, symbol, truth table and timing diagram.	8	(2 :3: 1.3.1)

OR

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| 6. | a. | Explain the application of SR latch as switch debouncer. | 6 | (2 :3: 1.3.1) |
| | b. | With the help of neat logic diagram and waveforms, explain positive edge triggered D flip flop. | 8 | (2 :3: 1.3.1) |
| | c. | Derive characteristics equations for SR flip flop, JK flip flop. | 6 | (2 :3: 1.3.1) |

MODULE – 4

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| 7. | a. | Explain SISO, SIOP shift operations with relevant diagrams. | 4 | (2 :4: 1.3.1) |
| | b. | Design universal shift register to perform following functions:
S1, S0 = Complement; S1, S0 = Hold;
S1, S0 = Shift right; S1, S0 = Parallel input. | 8 | (3 :4: 1.3.1) |
| | c. | Design 4-bit asynchronous UP counter using positive edge triggered T flip flop. | 8 | (3 :4: 2.1.2) |

OR

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| 8. | a. | Explain the Ring counter and Johnson counter and implement using 7495IC. | 8 | (2 :4: 1.3.1) |
| | b. | Derive the application tables for SR, JK, T and D Flip-Flops using next state tables. | 4 | (3 :4: 2.1.2) |
| | c. | Design synchronous MOD-8 counter using clocked D flip flop for the sequence 0→2→4→6→8→10→12→14→ again 0→2→ | 8 | (3 :4: 2.1.2) |

MODULE – 5

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| 9. | a. | Explain Moore and Mealy models with relevant block diagrams | 8 | (2 :5: 1.3.1) |
| | b. | Construct state table and state diagram for the following sequential circuit shown in fig. a. | 12 | (3 :5: 2.1.2) |

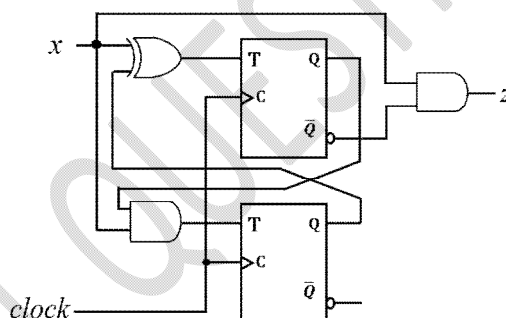


Fig. a

OR

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| 10. | a. | Explain state machine notations with examples and relevant diagrams. | 8 | (2 :5: 1.3.1) |
| | b. | A sequential circuit has one input and one output, the state diagram shown in fig.b, design sequential circuit using JK Flip Flops. | 12 | (3 :5: 2.1.2) |

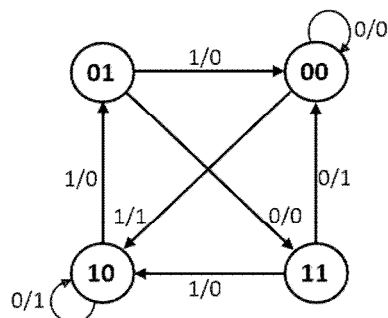


Fig. b

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