

Basavarajeswari Group of Institutions
BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT
 (Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN

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Course Code

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Third Semester B.E. Degree Examinations, March/April 2024

ANALOG ELECTRONIC CIRCUITS

Duration: 3 hrs

Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
 2. Missing data, if any, may be suitably assumed

| <u>Q. No</u> | <u>Question</u> | <u>Marks</u> | <u>(RBTL:CO:PI)</u> |
|-----------------|--|--------------|---------------------|
| Module-1 | | | |
| 1. | a. What is equivalent circuit? Sketch the equivalent circuits of diode for the following biasing conditions. (i) Ideal diode (ii) Piece wise linear model (iii) Approximate model | 06 | (2 : 1 : 1.3.1) |
| | b. Explain the working principle of FULL wave rectifier and prove that (i) Ripple factor $\gamma = 0.482$ (ii) Efficiency $\eta = 81.00\%$ | 08 | (2 : 1 : 1.3.1) |
| | c. Explain the positive and negative clamping circuits with neat waveform. | 06 | (2 : 1 : 1.3.1) |
| OR | | | |
| 2. | a. Explain construction and working principle of transistor with current/carrier flow diagram. | 06 | (2 : 1 : 1.3.1) |
| | b. Write a note positive fixed 78XX series voltage regulator and adjustable voltage regulator LM 317. | 08 | (2 : 1 : 1.3.1) |
| | c. Explain the construction and operation of depletion type of MOSFET and draw the drain and transfer characteristics. Explain the principle of operation of depletion MOSFET. | 06 | (2 : 1 : 1.3.1) |
| Module-2 | | | |
| 3. | a. What is biasing? Explain voltage classical voltage divider bias circuit and discuss the design equation with examples. | 08 | (2 : 2 : 1.3.1) |
| | b. Define small signal modelling and derive expression of collector current and trans conductance. | 08 | (2 : 2 : 1.3.1) |
| | c. Draw the hybrid T Model of transistor with necessary equations. | 04 | (2 : 2 : 1.3.1) |
| OR | | | |
| 4. | a. Explain biasing by fixing V_{GS} and connecting source resistance. | 06 | (2 : 2 : 1.3.1) |
| | b. Explain drain to gate feedback resistor biasing MOSFET | 06 | (2 : 2 : 1.3.1) |
| | c. Draw the small signal equivalent circuit model for MOSFET and obtain the expression for voltage gain. | 08 | (2 : 2 : 1.3.1) |
| Module-3 | | | |
| 5. | a. Explain the different configuration of MOSFET amplifier and characterization amplifier with necessary equation. | 10 | (2 : 3 : 1.3.1) |
| | b. Derive the input impedance, output impedance and voltage gain for the common source amplifier with source resistance | 10 | (2 : 3 : 1.3.1) |
| OR | | | |
| 6. | a. Draw the high frequency model of MOSFET and obtain simplified model with proper assumption. | 06 | (2 : 3 : 1.3.1) |

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI- Performance Indicator)

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| b. | Write a short note on current mirror and current steering circuit. | 08 | (2 :3: 1.3.1) |
| c. | Explain the three frequency bands in MOSFET CS-Amplifier. | 06 | (2 :3 : 1.3.1) |

Module-4

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| 7. | a. | Draw the block diagram of feedback amplifier and derive the overall gain with feedback. | 06 | (1 :4 : 1.3.1) |
| | b. | Explain the different topologies of feedback amplifier with neat block diagram. | 10 | (2 :4: 2.2.1) |
| | c. | List the properties of negative feedback. | 04 | (1 :4 : 1.3.1) |

OR

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| 8. | a. | Explain the working principle of class-A amplifier output stage and draw the transfer characteristics with necessary equations. | 10 | (2 :4 : 1.3.1) |
| | b. | Draw the class-B output stage circuit and prove that the efficiency of class B output stage efficiency is 78.5%. | 10 | (2 :4: 2.2.1) |

Module-5

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| 9. | a. | Explain instrumentation amplifier with bridge circuit diagram and derive equation for output voltage. | 08 | (2 :4: 1.3.1) |
| | b. | Briefly explain peak detector using op-amp with necessary waveform. | 06 | (2 :4: 1.3.1) |
| | c. | Explain the working principle of successive approximation network ADC. | 06 | (2 :4: 1.3.1) |

OR

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| 10 | a. | Design and explain the first order low pass butterworth filter with circuit diagram. | 06 | (2 :4: 1.3.1) |
| | b. | Explain the operation of 555 timer as an astable multivibrator with relevant expressions. | 08 | (2 :4: 1.3.1) |
| | c. | Design the astable multivibrator with the following specification. C=0.1μF (i) $f_o=1\text{kHz}$, Duty Cycle=40% (ii) $f_o=2\text{kHz}$, Duty Cycle=50% | 06 | (2 :4: 2.2.1) |

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