

National Level Faculty Development Program

Five Days Online FDP on  
**VLSI Design**  
For Beginners and Advanced Users

Registration

17<sup>th</sup> April to 21<sup>st</sup> April 2021



SCAN QR to register or visit  
[tinyurl.com/bitmvlisifdp](http://tinyurl.com/bitmvlisifdp)

Organizing Committee

Chief Patron

Dr. Yashvanth Bhupal , Director, BITM, Ballari

Patron

Prof. Prithviraj Y J, Dy. Director, BITM, Ballari

Dr. V C Patil, Principal, BITM, Ballari

Chairperson

Dr. U Eranna, HOD, Dept. of ECE, BITM, Ballari

Convener

Dr. Naseeruddin, Assoc. Prof. ECE Dept.

Resource Persons

1. K Mohammed Maaz  
Director (AMS Layout & Physical Verification )  
SEMIONICS Limited.
2. Chandra Sekhar Sakala  
Staff Engineer,  
Samsung.
3. Experts from Entuple Technologies

Workshop Committee

Teaching, Non-Teaching Staff Members & Students  
Volunteers of Electronics and Communication  
Engineering Department, BITM, Ballari

For more details visit our website:

[www.https://sites.google.com/view/.....](http://www.https://sites.google.com/view/.....)

**Note: The capacity is limited to 100 Participants only**

Five Days Online FDP on  
**VLSI Design**  
For Beginners and Advanced Users

National Level Faculty Development  
Program  
17<sup>th</sup> April to 21<sup>st</sup> April 2021



Organized by

Department of Electronics and  
Communication Engineering



Ballari Institute of Technology and  
Management

Jnana Gangotri Campus, Hosapete Road, Near  
Allipura, Ballari, Karnataka-583104

Approved by AICTE, New Delhi and Affiliated to  
VTU, Belgaum

## Workshop Objectives

## About Department

The Department of Electronics and Communication Engineering was established in the year 1997 with an intake of 40. Presently the intake is 180. It is one of the most sought branches of engineering & technology in the modern day. The Department has an efficient and dedicated team of staff who meticulously plan, train and guide the students in their academic activities, which motivates the students to achieve higher educational levels. The department conducts regular seminars & workshops in association with industry to equip the students with practical insight and help the students to incorporate these technologies into their specializations and achieve higher educational levels. The department conducts regular seminars & workshops in association with industry to equip the students with practical insight and help the students to incorporate these technologies into their specializations.

## About BITM

Ballari Institute of Technology & Management (BITM) was established in the year 1997 with the aim of providing quality education. The institution is run by TEHRD trust, Founded by Late Smt. Basavarajeshwari, Former Union Minister. The Institution is recognized by Govt. of Karnataka, approved by AICTE, New Delhi & affiliated to Visveswaraya Technological University, Belagavi. The Institution has been accredited by A+ by NAAC and is certified by ISO 9001:2015. BITM empowers the students with technical & Managerial skills, Professional ethics & values and appreciation of human creativity and innovation for an inquisitive mind. Its Place vital role in producing top quality professional to meet Industrial & Technological requirements.

## Contact Person

1. Mr. Raymond Irudayaraj I  
Asst. Professor, Dept. of ECE,  
BITM, Ballari.  
Ph. No: 9972803296  
Email Id: raymond.jhts@gmail.com

## Topics to be covered

### :Day1:

- Welcome to the world of CHIP Designing
- Analog and Mixed Signal Flow / Latest Technology Trends / Core Expertise

### :Day2:

- Fabrication technology overview
- Cost-performance trade-off
- Different layout types
- Chip Architecture
- Stick diagrams
- About Standard cell layout, Memory layout, Analog layout, IO layout
- Layout verifications
- Foundrys

## Topics to be Covered in the Workshop

### Day3: Full Custom Design Flow

- Introduction about VLSI
- MOSFET as capacitor, MOSFET VI characteristics,
- Schematic capture using Virtuoso
- Functional simulation Using Spectre
- Schematic Driven layout Design Using Virtuoso
- Layout editor
- Physical verification which includes DRC & LVS using Assura, Parasitic extraction, Post Layout Simulation
- Generation of GDSII, Lab Session for Participants

### Day4: Semi Custom Design Flow

- Functional Verification Flow using INCISIVI
- RTL synthesis using GENUES
- DFT flow Using GENUES & MODUS
- Logical Equivalence check using conformal
- Lab Session for Participants

### Day5: Semi Custom Design Flow

- TD flow which innovates that includes
  - ✓ Floor planning
  - ✓ Power planning
  - ✓ Placement
  - ✓ CTS
  - ✓ Routing
  - ✓ Generation of GDSII
- Post layout timing sign of using TEMPUS
- Power sign of using VOLTUS
- Lab Session for Participants

## WORKSHOP REPORT

Five day online FDP on “VLSI Design for Beginners and Advanced Users ” has been organised by the Department of Electronics and Communication Engineering for the faculty members. The objective of the workshop was to offer detailed hands on experience on various aspects of VLSI design using Cadence tools.

The program details are as follows:

1. Name of the event : **VLSI Design for Beginners and Advanced Users**
2. Dates : 17-04-2021 to 21-04-2021
3. Time : 10AM To 4:30 PM
4. Venue : EC Seminar Hall
5. Resource Persons : Mr. K Mohammed Maaz  
Director (AMS layout & physical verification)  
Mr. Chandra shekar sakala, staff Engineer Samsung  
Bengaluru.
6. Workshop Co-ordinator : Dr. Naseeruddin, Associate Professor ECE Dept.

### Objectives of the Workshop:

- To provide an industry-academia platform
- To enhance EDA tool usage skills relevant to the industry
- To realize the importance of adapting to ever changing needs of VLSI industry

### Outcome:

- Participants understood and given industry-academia platform.
- Participants have learnt EDA tool usage skills relevant to the industry
- Participants carried out various case studies to realize the importance of adapting to ever changing needs of VLSI industry

meet.google.com/vqx-mizq-hxp

Prathiba Shanbog and 5 more 10:16 AM You

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Go to Settings to activate Windows.  
Turn on captions Present now

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10:16 AM 4/17/2021

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K Mohammed Maaz is presenting sowubhagya bh... and 19 more 10:27 AM You

welcome to The World of Chip designing

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By: K Mohammed Maaz

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10:27 AM 4/17/2021

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10:28 AM

# Abstract

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- ▶ Foundry / EDA / Design House
- ▶ VLSI Design Flow
- ▶ Bridging Academia and Semiconductor Industry
- ▶ Do you have the Foundation needed ?
- ▶ Knowledge and skills we offer ! / Course Details
- ▶ Professional Value for Students/Faculty and College
- ▶ Over all Course in a Nutshell ...!
- ▶ Semiconductor companies
- ▶ Q & A

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NAGA V SATYANARAYANA M 16PHD... and 14 more

10:33 AM

# Electronic Design Automation companies

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- ▶ They Design the EDA tools used for Design , Analysis and Verification

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### VLSI Design Flow

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Suralatha M JRT... and 11 more

10:37 AM

K Mohammed Maaz

Raymond Irudayaraj

channaveera gouda

shiv kumar

Neela Guruswamy

simantini Roy royc...

Saravanan Siva

premachand dr

sindigi Manjunath

Raymond Irudayaraj

Ulaganathan Jayap...

Lokesh Ks

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### Bridging Academia and Semiconductor Industry

- Why Don't Companies Hire Electronics Engineers ?
  - Lack of Hands on skill
  - Companies/ colleges ,cannot afford to Train
  - Time to market is less
  - Industry Needs Plug & play resource .
- Bachelors / Diploma / BSc in E&C / EEE is a required
- What ever foundation I have , will it fetch me a Job in EEE/E&C domain ?
- What MORE Does it take to bridge the gap ?
  - Job Descriptions

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prabhu achar and 12 more

10:41 AM

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channaveera gouda

shiv kumar

Neela Guruswamy

simantini Roy royc...

Saravanan Siva

premachand dr

sindigi Manjunath

Raymond Irudayaraj

Ulaganathan Jayap...

Lokesh Ks

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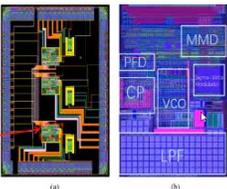
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10:47 AM

### What MORE Does it take to bridge the gap ?

**Job Requirement : " Analog Layout Engineer"**

- Understand CMOS Basics / basic Electronics / Analog / Electrical concepts / Digital
- Hands on experience on Analog /Mixed signal IC Layout design .
- Familiarity of PLL, OPAMP, BIAS , LDO , Amplifier , ADC, oscillator
- Should be experienced in 180nm, 90nm, 45nm, 28nm CMOS technologies .
- Should be familiar with usage of EDA tools / Cadence / Mentor Graphics / Virtuoso Layout Editor / Calibre
- Familiar with Linux environment , Quick learner , good in communication



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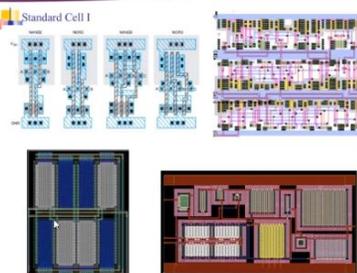
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10:51 AM

### Course: LAB Assignments and Project Work

- Full Custom layout Lab
- Standard Cell Digital Layout lab
- Combinational / Sequential Logic Layout
- Analog Layout Lab work
- Matching concepts
- High speed / High Current Layout concepts
- OPAMPS / Level shifters / Voltage Dividers
- Flash ADC / Power switches ( Project work )
- Physical Verification Flows ( DRC /LVS )
- Many More .....



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Prathiba Shanbog and 15 more

10:57 AM

### Semiconductor companies

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```

    graph TD
      A[Types of VLSI companies] --> B[Product Company]
      A --> C[Service Company]
      B --> D[EDA Company]
      B --> E[Design Company]
      F[EDA companies Job Roles] --> G[RnD Engineer]
      F --> H[Product Engineer]
      F --> I[Product validation Engineer]
      F --> J[Application Engineer]
  
```

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Mallikarjun Naidu and 16 more

10:59 AM

### some of product companies

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- Texas Instruments
- Broadcom
- Intel
- Qualcomm
- NXP
- ST Microelectronics
- Samsung
- AMD
- ARM
- NVIDIA
- Global Foundries
- Siemens
- Many More

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Session 2

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People (17)

- Saravanan Siva
- Seema SRIVASTAVA
- shiv kumar
- simantini Roy roychowd...
- sindigi Manjunath
- Sumalatha N
- Ulaganathan Jayapal
- Vijaya H

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1:48 PM 4/17/2021

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K Mohammed Maaz is presenting

1:38 PM You

AGENDA

- ▶ The Fast World
- ▶ Mixed Signal Flow
- ▶ Single Verification Platform
- ▶ Comprehensive Technology
- ▶ Nature of Designs
- ▶ Mixed Signal Data Flow
- ▶ Latest Technology trends
- ▶ Core Expertise needed
- ▶ Q & A

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Watch Uyanis Buyuk Selcuklu wi... | Watch Uyanis Buyuk Selcuklu Sei... | VLSI design FDP - 2nd Session | | Meet - vqx-mizq-hxp

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Sacloyjatha k.m. and 1 more

1:42 PM

Show everyone

### The Fast World

"GATE-LEVEL" HIGH-K/METAL GATE ESTIMATION

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Anitha K and 6 more

1:42 PM

### MIXED SIGNAL FLOW

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1:42 PM

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srikanth k.m and 7 more

You

# Comprehensive Technology

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**Digital System-Level**

- VHDL
- Verilog
- ModelSim/Questa

**Analog Mixed-Signal**

- VHDL-AMS
- Verilog-AMS

**SPICE Physical-Device**

- ADiT
- Eldo
- Eldo RF

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JAVALKAR VINAY and 5 more

You

# Comprehensive Technology

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**ADVANCE mS**

**Digital System-Level**

- VHDL
- Verilog
- ModelSim/Questa

**Analog Mixed-Signal**

- VHDL-AMS
- Verilog-AMS

**SPICE Physical-Device**

- ADiT
- Eldo
- Eldo RF

**Mixed-Signal SoC Functional Verification**

- Digital Logic
- AMS IP Memory and Custom Logic
- Analog
- RF

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PREMACHAND ... and 7 more

## NATURE OF THE DESIGNS

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HOW DO WE DO IT ? ! semionics@gmail.com

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Nilam Chheda and 3 more

## MIXED SIGNAL DATA FLOW

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srikanth k.m and 5 more

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## HANDLING SENSITIVE SIGNALS / DIFFERENTIAL NETS

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- ▶ shielding
  - ❖ Side wall shielding
  - ❖ Co-axial shielding
- ▶ Differential Routing
  - ❖ Match Trace lengths
  - ❖ Reduce separation between traces
  - ❖ Maintain matched impedance

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srikanth k.m and 5 more

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## SCHEMATIC DESIGNER

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- ▶ Circuit Design / Functional Simulation
- ▶ Process Corner simulations ( Process / Voltage / Temperature )
- ▶ EM/IR Simulation Etc
- ▶ Ageing Simulation

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Differential Amplifier with Current Source.

Fig 9. AC response of the Differential Amplifier with Current Source.

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PREMACHAND ... and 4 more

17 You

# LAYOUT DESIGNER

- ▶ Layout Design
- ▶ Matching Techniques
- ▶ Latchup
- ▶ Signal Integrity / Shielding
- ▶ EM / IR
- ▶ Power Mesh Creation
- ▶ High speed Layout techniques
- ▶ Handling clocks
- ▶ High Current designs

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sindigi Manjunath and 5 more

18 You

# PHYSICAL VERIFICATION ENGINEER

- ▶ DRC ( Design Rule Check )
- ▶ LVS ( Layout Vs Schematic Check )
- ▶ ERC ( Electrical Rule Check )
- ▶ ANT ( Antenna Rule Check )
- ▶ DENSITY ( Density Rule Checking )
- ▶ DFM ( Design For Manufacturability )
- ▶ LFD ( Litho Friendly Design )
- ▶ LCC ( Layout Compliance Check )
- ▶ IP Closure checks

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**CYCLE OF A CHIP**

Design → Design → Design → Design → Design

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People (16) Chat

You 2:36 PM  
Dear Participants, Kindly provide your valuable feedback for the 1st Day of FDP, Link will be shared shortly in chat box

Send a message to everyone

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Watch Uyanis Buyuk Selcuklu x Watch Uyanis Buyuk Selcuklu x VLSI design FDP - 2nd Session x Meet - vxq-mizq-hxp Feedback DAY-1 (FDP on VLSI) x

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PREMACHAND ... and 1 more

2:40 PM

You are presenting

Stop presenting

Meeting details

Meeting details

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Day 2: From Sakala

Day 3:

Ultrasurf - Top Stories x VLSI Design FDP Day-3,4,5 link x Meet - nfq-kops-bdz x Watch Uyanis Buyuk Selcuklu x Watch Uyanis Buyuk Selcuklu x

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S Sagar hb is presenting 13 10:16 AM You

## About Entuple

**ENTUPLE TECHNOLOGIES**

- Design Service, Product and Engineering Solution Provider in cutting edge technologies
  - Electronic System Design, VLSI/Semiconductor, Electrical Drives & Renewable Energy Systems, RF & Antenna, Additive Manufacturing, Mechanical, Finite Element Analysis (FEA), Computational Fluid Dynamics, PCB Design & Prototyping Solutions, IoT & Data Sciences and more
- Our customer base
  - Aerospace & Defence, Mid Market - Design and Product Development Houses in multiple technology verticals, Multinational Technology Leaders, Original Equipment Manufactures (OEMs), R & D Organizations & Academia.

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S Sagar hb is presenting 14 10:17 AM You

## Domains

**ENTUPLE TECHNOLOGIES**

 Mechanical	 CFD	 EMAG	 Systems	 Semiconductors
 eMobility	 PCB Design	 PCB Proto	 3D Printing	 Indented Test
 VNA	 RF Solutions	 Cyber Security	 Internet of Things	 Power Electronics

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## Entuple - A bird's eye view

ENTUPLE TECHNOLOGIES

**Quick Facts**

- Incorporated - 01.01.10
- HQ - Bangalore
- RO - NCR Delhi, Pune, Ahmedabad, Hyderabad
- Total No. of Offices - 13
- Team Size - 135

**Customers**

- A & D - 30
- MSME & Mid - 15
- RBU - 10
- Academia - 300

**Staff split**

- Sales - 35
- Technical - 75
- Administrative - 10

INDIA  
OUTLINE MAP WITH STATES

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## Ground up from the Basics (01/03)

### Information Acquisition, Processing and Transaction

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$D(t) = d1d0 = 10$   
 $D(t) = d1d0 = 06$   
 $D(t) = d1d0 = 00$

$D(t) = d1d0 = 10$   
 $D(t) = d1d0 = 06$   
 $D(t) = d1d0 = 00$

**Observe:**

- We use numbers to quantify and compare
- Decimal number system → most natural to us!
- Discrete / Discreet?!
- Discrete → individual, distinct
- Contextually → a judicious choice
- Discreet → Guarded, close mouthed.
- Discontinuous → Digital !!
- Not a function of the number system in use!
- So Why Use Binary for Digital?
- Decimal → Every digit can exist in any of the 10 possible distinct levels
- Cumbersome to build such systems
- Therefore, say good bye to (2, 3, ...9)!!
- Binary!!

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Nilam Chheda and 4 more

### Quality Metrics of a Digital Gate (01/04) ENTUPLE TECHNOLOGIES

Question 1: How robust is the gate?

- What are the **guaranteed** output voltage levels for "0" and "1"?
  - $V_{OH}, V_{OL}$
- What are the **worst case** input logic levels for which the gate produces the corresponding guaranteed output logic levels?
  - $V_{IL}, V_{IH}$
- What are the worst case **noise** amplitudes the gate is able to overpower and provide functionally correct responses?
  - Noise Margins**
    - $NMH = V_{OH} - V_{IH}$
    - $NML = V_{IL} - V_{OL}$

Truth Function Table (Example):

A	Y
0	1
1	0

Practical VTC vs Ideal VTC graph showing  $V_{OH}, V_{OL}, V_{IH}, V_{IL}$  and  $Slope = -1$ .

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Abdul Samad and 5 more

### Quality Metrics of a Digital Gate ENTUPLE TECHNOLOGIES

Question 2: How fast is the gate response?

- $t_{pd,r}$ : rising propagation delay
  - From input to rising output crossing  $V_{DD}/2$
- $t_{pd,f}$ : falling propagation delay
  - From input to falling output crossing  $V_{DD}/2$
- $t_{pd,a}$ : average propagation delay
  - $t_{pd,a} = (t_{pd,r} + t_{pd,f})/2$
- $t_r$ : rise time
  - From output crossing  $0.2 V_{DD}$  to  $0.8 V_{DD}$
- $t_f$ : fall time
  - From output crossing  $0.8 V_{DD}$  to  $0.2 V_{DD}$

Truth Function Table (Logical):

A	Y
0	1
1	0

Timing diagram showing  $t_{pd,r}, t_{pd,f}, t_{pd,a}, t_r, t_f$ .

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Saravanan Siva and 4 more

10:56 AM

### MOSFET as a Capacitor (01/04) ENTUPLE TECHNOLOGIES

- MOSFET as a Capacitor: Accumulation
  - $v_G < 0, v_S = v_D = v_B = 0$
  - Majority carriers accumulate @ Si - SiO<sub>2</sub> interface!
  - Surface hole density,  $p_{p,s}$
  - Bulk hole density,  $p_{p0,b}$
- MOSFET in Accumulation
  - $\psi_s < 0$
  - Maj. Carrier Accumulation
- MOSFET as a Capacitor: Depletion
  - $0 < \psi_s < \psi_{s0} \Rightarrow \psi_s = \psi_b = 0$
  - As  $\psi_s$  increases above zero volts
  - Positive charge on the metal electrode repels holes under SCG
  - Leaves behind a layer of negative ions
  - Depletion region under SCG
  - No carriers exist in the depletion region (indefinite!)

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Naga satyanarayana mu... and 6 more

11:05 AM

### The Inverter – A Quick Recap! ENTUPLE TECHNOLOGIES

Truth Function Table (Boolean)

A	Y
0	1
1	0

Practical VTC

Minid VTC

Slope = -1

CURRENT SINK INVERTER

CURRENT SOURCE INVERTER

PUSH-PULL INVERTER

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Meet - nfq-kops-bdz

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Sagar hb is presenting

Neela Guruswa... and 7 more

11:12 AM

Applications Places Log: /root/CDS.log

root@cadence:BIT\_workshop

```
File Edit View Search Terminal Help
Welcome to Cadence Tools Suite
[root@cadence BIT_workshop]# virtuoso &
[1] 24333
[root@cadence BIT_workshop]#
```

Virtuoso 6.1.7-64b - Log: /root/CDS.log

Meeting details

Activate Windows

Turn on captions

Go to Settings to activate Windows. Sagar hb is presenting

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anu a and 9 more

11:16 AM

Applications Places Virtuoso Schematic Editor: Editing: workshop.bit\_inverter.schematic

Virtuoso Schematic Editor 1

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Sagar hb is presenting

Meeting details

People (23)

- Prema Chand D R
- Sagar hb
- Sagar hb Presentation
- Saravanan Siva
- shilpa chetan
- sowubhagya bhagya
- Ulaganathan Jayapal
- Veeresh K M

Meeting controls: Mute, Unmute, End Meeting

Windows taskbar: Type here to search, 11:52 AM 4/19/2021

## Day 4

Meet - nfq-kops-bdz

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Sagar hb is presenting

10:10 AM

Meeting details

People (23)

- You
- Sagar hb
- Ramchandra K Gurav
- Hiremathada Shivabasav...
- Manjunath Ganjipete
- srikanth k.m
- Ulaganathan Jayapal
- Raymond Irudayaraj

Meeting controls: Mute, Unmute, End Meeting

Windows taskbar: Type here to search, 10:10 AM 4/20/2021

Meet - nfq-kops-bdz

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Sagar hb is presenting

Raymond Iruday... and 2 more

10:35 AM

Applications Places NCLaunch /root/Desktop/digital\_ext/functional\_verification

Browser: /root/Desktop/digital\_ext/functional\_verification

Directory: /root/Desktop/digital\_ext/functional\_verification

worklib  
counter  
counter\_test  
snapshots  
worklib\_counter\_module  
worklib\_counter\_test\_module

cadence

Simulation Analysis Environment  
SimVision(64) 15-20-s051

Loading Default layout.

Intel(R) Xeon(R) Processor E5-2680 v4  
System Memory 16 GB  
Copyright (C) 1985-2018 Cadence Design Systems, Inc.

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Go to Settings to activate Windows.

Sagar hb is presenting

Meet - nfq-kops-bdz

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Sagar hb is presenting

10:41 AM

Applications Places LibreOffice 7.1 Impress

Synthesis(Genus) LibreOffice Impress

File Edit View Insert Format Slide Slide Show Tools Window Help

Slides

Agenda

- Introduction to Semi Custom IC Design (ASIC Flow)
- Introduction to Synthesis
- Introduction to Genus Synthesis Solution Tool
- A Brief Insights of .jil, .lef and connecting with RTL and SDC files
- A Brief description of Gate Level Netlist
- Performing RTL Synthesis flow
- Report Analysis for Power Performance Area (PPA)

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Meeting details

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Sagar hb is presenting

10:43 AM

**ASIC Design Flow**

```

    graph TD
      START([START]) --> SPEC[SPECIFICATION]
      SPEC --> RTL[RTL CODING]
      RTL --> INC[INCISIVE]
      INC --> FUS[FUNCTIONAL SIMULATION]
      FUS --> GEN[GENUS]
      GEN --> SYN[SYNTHESIS]
      SYN --> MOD[MODUS]
      MOD --> DFT[DFT]
      DFT --> FLOOR[FLOORPLANNING]
      FLOOR --> PPL[POWER PLANNING]
      PPL --> PL[PLACEMENT]
      PL --> CTS[CTS]
      CTS --> ROUT[ROUTING]
      ROUT --> GDS[GDS II]
  
```

ENTUPLE TECHNOLOGIES

INNOVUS

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Slide 4 of 24

Meeting details

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Sagar hb is presenting

11:06 AM

**Start of Genus Tool**

- To launch genus:
  - linux:/> genus -legacy\_ui
- Genus could be launched in batch mode with .tcl script
  - genus -legacy\_ui -f genus\_script.tcl
- By default, the GUI is not visible
  - legacy\_genus:/> gui\_show
  - legacy\_genus:/> gui\_hide

ENTUPLE TECHNOLOGIES

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Slide 17 of 24

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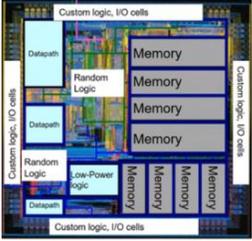
S Sagar hb is presenting

11:42 AM

ENTUPLE TECHNOLOGIES

## Conformal Product Family

- Conformal L (ASIC) Equivalence Checker (EC)**
  - Verifies synthesized and place and route netlist transformations
- Conformal XL (Ultra) Equivalence Checker**
  - Conformal L +
  - Verifies complex datapath
- Conformal GXL (Custom) Equivalence Checker**
  - Conformal XL +
  - Verifies custom logic, I/O cells, custom memories, standard libraries
  - Verifies final LVS netlist
- Conformal Low Power**
  - Conformal XL +
  - Verifies low-power logic
  - Verifies power domains



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11:49 AM

S Sagar hb is presenting

11:49 AM

ENTUPLE TECHNOLOGIES

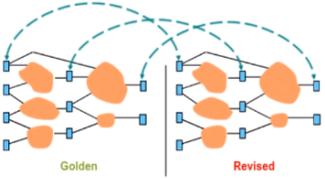
## What Is Mapping?

During equivalence checking you read in two designs to compare them.

- The design you are comparing against must be considered Golden.
- The modified must be considered Revised.

Mapping is pairing corresponding Golden and Revised key points.

<b>Golden</b>	← →	<b>Revised</b>
PI	← →	PI
PO	← →	PO
DFF	← →	DFF
DLAT	← →	DLAT
BBOX	← →	BBOX
CUT	← →	CUT
Z	← →	Z
E	← →	E



Key points  
Combinational logic

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ENTUPLE TECHNOLOGIES

## How to Start and Exit Conformal LEC

**Start**

To start the Equivalence Checker use `lec`.

To get help on all the options use `lec -help`.

**Exit**

To exit Conformal LEC: `exit [-force]`

LEC automatically closes all windows upon exit.

**Starting Conformal® LEC**

- Menu mode: `lec [-L] -XL | -GXL | -ECO | -LPLX | -LPGXL]`
- Command mode: `lec [-L] -XL | -GXL] -nogui //Then run dofile <command_file>`
- Switch between menu and command modes: `set gui [on | off]`
- Batch mode: `lec -dofile <batch_file> -nogui`

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12:23 PM

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Tempus PPT, Office Impress

File Edit View Insert Format Slide Show Tools Window Help

Slides

EXCEL VLSI

## Delay

ENTUPLE TECHNOLOGIES

- Delay is the time taken by a signal to change state or propagate from one point to another in a circuit.
- There are two types of Delay
- Cell delay
  - Intrinsic delay or self delay for no load on output
  - Cell delay/gate delay/propagation delay for a given input slew and output load; already discussed in previous session
  - Slew or Transition time at output for a given input slew and output load; already discussed in previous session
- Wire delay
  - Delays due to parasitics on net/wire also called Net Delay/Interconnect delay/Extrinsic delay/Flight time

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Slides

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EXCEL VLSI Slack ENTUPLE

- Slack is defined as difference between actual or achieved time and the desired time for a timing path.
- Slack determines if the design is working at the specified speed or frequency for a particular timing path.
- Timing and slack definitions :
  - Arrival time - The time taken by the data to travel to the end point.
  - Required time - The time required for the data to travel to the end point.
  - Slack = Required time - Arrival time
  - Positive Slack - Arrival time is before the required time
  - Negative Slack - Arrival time is after the required time.
  - Zero Slack - Arrival time and Required time are same.
- Positive slack and zero slack are called as "Timing met"

Slide 28 of 35

Meeting details

12:36 PM

You Sagar hb channaveera ... Hiremathada ... Anitha K ECE is EASY#... Nilam Chheda Ulaganathan ... srikanth k.m

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Slides

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34

35

EXCEL VLSI Example of REG2REG timing slack ENTUPLE

$T_{su} = 0.1ns, T_h = 0.2ns$   
Clock period = 2ns

Gate	Cell delay
BuF	0.1
FF1	0.2
FF2	0.3

Setup slack:  
Arrival time :  $0.2 + 0.1 = 0.3$   
Required time :  $2 - 0.1 = 1.9$   
Slack =  $R.T - A.T = 1.9 - 0.3 = 1.6ns(MET)$

Hold slack:  
Arrival time :  $0.2 + 0.1 = 0.3$   
Required time :  $0.2$   
Slack =  $A.T - R.T = 0.3 - 0.2 = 0.1ns(MET)$

Slide 34 of 35

Meeting details

12:41 PM

You Sagar hb channaveera ... Hiremathada ... Anitha K ECE is EASY#... Nilam Chheda Ulaganathan ... srikanth k.m

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Day 5

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PREMACHAND ... is also here

10:19 AM

```

root@cadence:Tempus_ext
File Edit View Search Terminal Help
tempus 1> read lib /home/ins
install/ install rb 22 08 2018 tar.gz
tempus 1> read lib /home/install/FOUNDRY/dig
digital.tar.gz digital/
tempus 1> read lib /home/install/FOUNDRY/digital/90nm/dig/lib/slow
slow.lib slow.lib ecm
tempus 1> read lib /home/install/FOUNDRY/digital/90nm/dig/lib/slow.lib
Scheduling timing library file(s) "/home/install/FOUNDRY/digital/90nm/dig/lib/s
low.lib" to be loaded when the set_top_module command is issued
tempus 2> read verilog ../
tempus ext/ functional_verification/ lec_ext/ logical_synth/
tempus 2> read verilog ../logical_synth/
constraints.top.sdc counter_netlist.v counter_tool.sdc fv/ genus.cmd
genus.log
tempus 2> read verilog ../logical_synth/co
constraints.top.sdc counter_netlist.v counter_tool.sdc
tempus 2> read verilog ../logical_synth/counter_netlist.v
Scheduling netlist file(s) "/logical_synth/counter_netlist.v" to be loaded whe
n the set_top_module command is issued
tempus 3> read sd
read sdc read sdt
tempus 3> read sdc ../
tempus ext/ functional_verification/ lec_ext/ logical_synth/
tempus 3> read sdc ../

```

Meeting details

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VLSI Design FDP Day-3,4,5 link - x Meet - nfq-kops-bdz

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Sagar hb is presenting

JAVALKAR VINAY and 2 more

10:21 AM

```

root@cadence:Tempus_ext
emulate_rc_corner
sius
: 1
: 1
: 1
emulate_rc_corner
sius
: 1
: 1
: 1

```

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VLSI Design FDP Day-3,4,5 link - x Meet - nfq-kops-bdz

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Sagar hb is presenting

PREMACHAND ... is also here

10:22 AM

```

root@cadence:~/tempus_ext# report_timing
# OS: Linux x86_64 (Host ID cadence)
# Generated on: Wed Apr 21 10:23:17 2021
# Design: counter
# Command: report_timing
#####
# Design Name: counter
# Design Mode: 65nm
# Analysis Mode: MWC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=694.486)
SAE DB initialization (MEM=713.464 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=817.395 CPU=0:00:00.0 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=809.395 CPU=0:00:00.3 REAL=0:00:01.0)
No constrained timing paths found.
Design may not be constrained or library is missing timing information.

tempus 6> set_design_mode -process 90
tempus 7>

```

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VLSI Design FDP Day-3,4,5 link - x Meet - nfq-kops-bdz

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Sagar hb is presenting

10:28 AM

```

root@cadence:~/tempus_ext# report_timing
#####
# Design Name: counter
# Design Mode: 98nm
# Analysis Mode: MWC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=792.746)
End delay calculation (fullDC). (MEM=826.512 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=826.512 CPU=0:00:00.1 REAL=0:00:00.0)
Path 1: REF Late External Delay Assertion
Endpoint: count[0] (?) checked with leading edge of 'clk'
Beginpoint: count_reg[0]/0 (^) triggered by leading edge of 'clk'
Path Groups: (clk)
Other End Arrival Time
- External Delay 1.000
- Phase Shift 2.000
- Required Time 1.000
- Arrival Time 0.474
- Slack Time 0.526
  Clock Rise Edge 0.000
  + Clock Network Latency (Ideal) 0.000
  = Beginpoint Arrival Time 0.000
-----
Instance Arc Cell Delay Arrival Required
Time Time
-----
count_reg[0] CK ^ 0.000 0.000 0.526
count_reg[9] CK ^ -> 0 ^ DFFRX1 0.474 0.474 1.000
- count[0] ^ - 0.000 0.474 1.000
-----
tempus 19>

```

Meeting details

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11:14 AM

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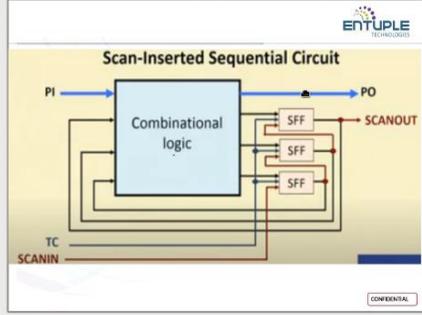
meet.google.com/nfq-kops-bdz

Sagar hb is presenting

11:15 AM

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- ### Why? The Chip Design Flow
- (continued)
- |  |   |
|--|---|
| <p>Reducing the level of abstraction:</p> <ul style="list-style-type: none"> <li>Customer requirements</li> <li>Specification</li> <li>Architecture</li> <li>Hardware description language</li> <li>Gates and nets</li> <li>Transistors, wires, and vias</li> <li>Shapes</li> </ul> <p>Building the chip:</p> <ul style="list-style-type: none"> <li>Masks</li> <li>Etches, diffusions, and depositions</li> <li>Dicing and packaging</li> </ul> | <p>Verifying the steps:</p> <ul style="list-style-type: none"> <li>Assertion/transaction checking</li> <li>Various types of simulation</li> <li>Formal (Boolean) verification</li> <li>Timing verification</li> <li>Shapes checking</li> <li>Optical inspection</li> <li>Wafer tests</li> <li>Module tests</li> </ul> |
|--|---|
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review.odg Libre Impress

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Slides

4  
5  
6  
7  
8  
9

Slide 6 of 27

Meeting details

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Sagar hb is presenting

Applications Places Innovus(TM) Implementation System 17.12 - /root/Desktop/digital\_extp...

Innovus(TM) Implementation System 17.12 ktop/digital\_ext/physical\_design - counter

File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help

Layout

Layers

Instance

- Type
- Block
- SlotCell
- Cover
- Physical
- ID
- Area IO
- Black Box

Function

- Status

Module

- Cell
- Blockage
- Row
- Floorplan
- Partition
- Power
- Overlay
- Track
- Net
- Route
- Layer
- Poly(G)
- Cont(O)

Detail

Speed

0 0.63700, 8.76300 In Memory

Meeting details

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Sagar hb is presenting

ECE is EASY#SUDHARSHAN BANA... is also here

12 You

LibreOffice 7.1 Impress

Innovus(TM) Implementation System 17.12

ktop/digital\_ext/physical\_design - counter

File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help

Layout

All Colors

- Instance
  - Type
    - Block
    - instCell
    - Cover
    - Physical
    - ID
    - Area ID
    - Black Box
  - Function
  - Status
- Module
- Cell
- Blockage
- Row
- Floorplan
- Partition
- Power
- Overlay
- Track
- Net
- Route
- Layer
  - Poly(0)
  - Core(0)

click the next point of the ruler.

review.odp - LibreOffice Impress

[root@cadence:physical\_design]

Innovus(TM) Implementation Syste...

2.51750, -1.41550 In Memory

1 / 4

Meeting details ^

Turn on captions

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Activate Windows  
Go to Settings to activate windows.

More options

S

Meeting - nfq-kops-bdz

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Sagar hb is presenting

```

root@cac ~# cat .design
= Beginpoint Arrival Time 0.000
-----
| Instance | Arc | Cell | Delay | Arrival | Required |
|-----|-----|-----|-----|-----|-----|
| count_reg[2] | CK ^ | SDFFRHX1 | 0.399 | 0.000 | 1.300 |
| count_reg[2] | CK ^ -> Q ^ | SDFFRHX1 | 0.399 | 0.399 | 1.759 |
| count_reg[2] | D ^ | SDFFRHX1 | 0.000 | 0.399 | 1.759 |
-----
Path 12: MET Setup Check with Pin count_reg[0]/CK
Endpoint: count_reg[0]/D (*) checked with leading edge of 'clk'
Beginpoint: count_reg[0]/QN (*) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: wc
Other End Arrival Time 0.000
Setup 0.155
Phase Shift 2.000
CPRR Adjustment 0.000
Uncertainty 0.010
Required Time 1.835
Arrival Time 0.451
Slack Time 1.384
Clock Rise Edge
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time 0.000
-----
| Instance | Arc | Cell | Delay | Arrival | Required |
|-----|-----|-----|-----|-----|-----|
| count_reg[0] | CK ^ | DFFR2 | 0.451 | 0.451 | 1.835 |
| count_reg[0] | CK ^ -> QN ^ | DFFR2 | 0.451 | 0.451 | 1.835 |
| count_reg[0] | D ^ | DFFR2 | 0.000 | 0.451 | 1.835 |
-----
Innovus >
  
```

Meeting controls: Mute, Video Off, End Meeting

Participants: You, Sagar hb, Nilam Chheda, Ulaganathan Jayapal

Meeting details

Windows taskbar: 2:25 PM 4/21/2021

Browser: meet.google.com/nfq-kops-bdz

Sagar hb is presenting

```

root@cac ~# cat .design
= Beginpoint Arrival Time 0.000
-----
| Instance | Arc | Cell | Delay | Arrival | Required |
|-----|-----|-----|-----|-----|-----|
| count_reg[2] | CK ^ | SDFFRHX1 | 0.399 | 0.000 | 1.300 |
| count_reg[2] | CK ^ -> Q ^ | SDFFRHX1 | 0.399 | 0.399 | 1.759 |
| count_reg[2] | D ^ | SDFFRHX1 | 0.000 | 0.399 | 1.759 |
-----
Path 12: MET Setup Check with Pin count_reg[0]/CK
Endpoint: count_reg[0]/D (*) checked with leading edge of 'clk'
Beginpoint: count_reg[0]/QN (*) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: wc
Other End Arrival Time 0.000
Setup 0.155
Phase Shift 2.000
CPRR Adjustment 0.000
Uncertainty 0.010
Required Time 1.835
Arrival Time 0.451
Slack Time 1.384
Clock Rise Edge
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time 0.000
-----
| Instance | Arc | Cell | Delay | Arrival | Required |
|-----|-----|-----|-----|-----|-----|
| count_reg[0] | CK ^ | DFFR2 | 0.451 | 0.451 | 1.835 |
| count_reg[0] | CK ^ -> QN ^ | DFFR2 | 0.451 | 0.451 | 1.835 |
| count_reg[0] | D ^ | DFFR2 | 0.000 | 0.451 | 1.835 |
-----
Innovus > saveD
Innovus > saveDesign
Innovus > saveDrc
Innovus > saveDesign route.enc -verilog
  
```

Meeting controls: Mute, Video Off, End Meeting

Participants: You, Sagar hb, Nilam Chheda, Ulaganathan Jayapal

Meeting details

Windows taskbar: 2:27 PM 4/21/2021

Browser: meet.google.com/nfq-kops-bdz

Sagar hb is presenting

Meeting controls: Mute, Video Off, End Meeting

Participants: You, Sagar hb, Nilam Chheda, Ulaganathan Jayapal

**PARTICIPANT LIST OF VLSI DESIGN FOR BEGINNERS AND ADVANCED USERS**

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9	K Ramchandra Kisan Gurav	ramgurav1987@gmail.com
10	Shilpa KR	shilpahitnalli2@gmail.com
11	Srikantha KM	sri.kanti87@gmail.com
12	Sumalatha	sumalathan27@gmail.com
13	vishnu Kanth Karwa	vishnukarwap@gmail.com
14	Prabhakark	prabhakarkachar@gmail.com
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20	HM Veeresh	riterulz@gmail.com
21	KM Spoorthi	spoorhi6@gmail.com
22	BR Neela	neela_guruswamy@jssateb.ac.in
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Recognized by Govt. of Karnataka, Approved By AICTE New Delhi and Affiliated to VTU, Belgaum

National level faculty development program

## **Certificate of participation**

This is to certify that

**Prof. SAGARA T V**

of BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT, BALLARI  
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**17<sup>th</sup> – 21<sup>st</sup> April 2021**

**Dr. Naseeruddin**  
**CONVENER**

**Dr. U Eranna**  
**HOD**

**Dr. V C Patil**  
**PRINCIPAL**

# Programme Schedule

Date	Time	Topic	Links
04/03/2021	2 pm to 3pm	Indian economy road ahead	<a href="https://meet.google.com/vsu-hqzg-hkm">https://meet.google.com/vsu-hqzg-hkm</a>
05/03/2021		Mutual funds for wealth creation	<a href="https://meet.google.com/ggx-pchp-jab">https://meet.google.com/ggx-pchp-jab</a>
06/03/2021		Indian economy post COVID 19	<a href="https://meet.google.com/ktd-vmrs-pho">https://meet.google.com/ktd-vmrs-pho</a>

## About: BSE Brokers' Forum

BSE Brokers' Forum formed in 1993 represents the concerns of the trading members in front of the Regulators and the Stock Exchanges. The Forum has been actively working for the betterment of the capital market in general and trading members in particular. The Forum has taken a project to spread the Financial Inclusion and Financial Literacy in association with the BSE IPF.

## Rules and Regulation

- Registration through link provided in brochure is mandatory
- Join the whatsapp group after successful registration
- The meeting Link shared in the e-brochure
- The number of participants is limited to 100 only.
- Platform: Google meet.
- E Certificate will be provided to those participants who attend all the 3 days program and attend MCQ and fill feedback form

## ABOUT BITM-DMS

Ballari Institute of Technology and Management- Department of Management Studies (DMS) was established in the year 2007 and affiliated to 'VTU Belgaum', and is a ISO 9001-2015 certified, CRISIL B-school 'KA B\*\*\*' graded, NAAC 'A+' accredited.

## BITM-DMS Recent Achievements



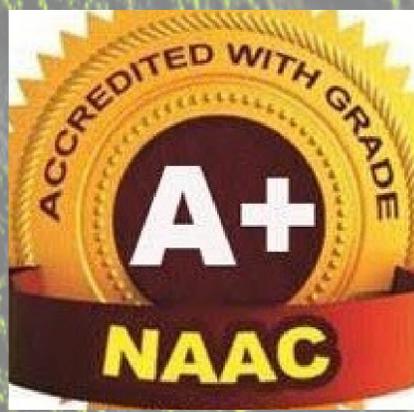
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# 3 day FDP Webinar Invitation

**Topic: Investing with Confidence during Pandemic**

**Date :March 4-6, 2021**

**Timing 2pm - 3pm.**

**Registration link**

**<https://forms.gle/WXrzRHya5hfeVJt7>**

**Our Speaker**



**Dr.V.Aditya Srinivas**

**Chief Operating Officer & Chief Economist  
Bombay Stock Exchange Brokers Forum, Mumbai**

**Ballari Institute of Technology & Management  
Department of Management Studies**

**In association with**

**IQAC Cell, FinWhiz Student Club &  
Bombay Stock Exchange Brokers Forum Mumbai**

**Event Coordinators**

**Dr Janet Jyothi Dsouza  
Associate Professor**

**Mr .Dinesh K  
Asst Professor**

# FDP REPORT

Three day faculty Development Program on “Investing with Confidence during Pandemic” has been organized by the Department of Management studies in association with Bombay Stock Exchange Brokers Forum Mumbai and IQAC Cell, Fin Whiz Student Club for the faculty members across the world through the online mode. The program details are as follows:

**Name :** Investing with Confidence during Pandemic

**Date :** 04/03/2021-06/03/2021

**Time :** 2 pm-3pm

**Venue/Mode:** online mode (Google Meet)

**Resource Person:** Dr.V. Aditya Srinivas Chief Operating Officer & Chief Economist Bombay Stock Exchange Broker

**Event Co-coordinator:** Dr Janet Jyothi D’Souza & Dinesh K

## *Objective of the Event*

- 1) To understand the role of financial planning for prospective investors
- 2) To identify the various emerging investment options suitable during economic crisis

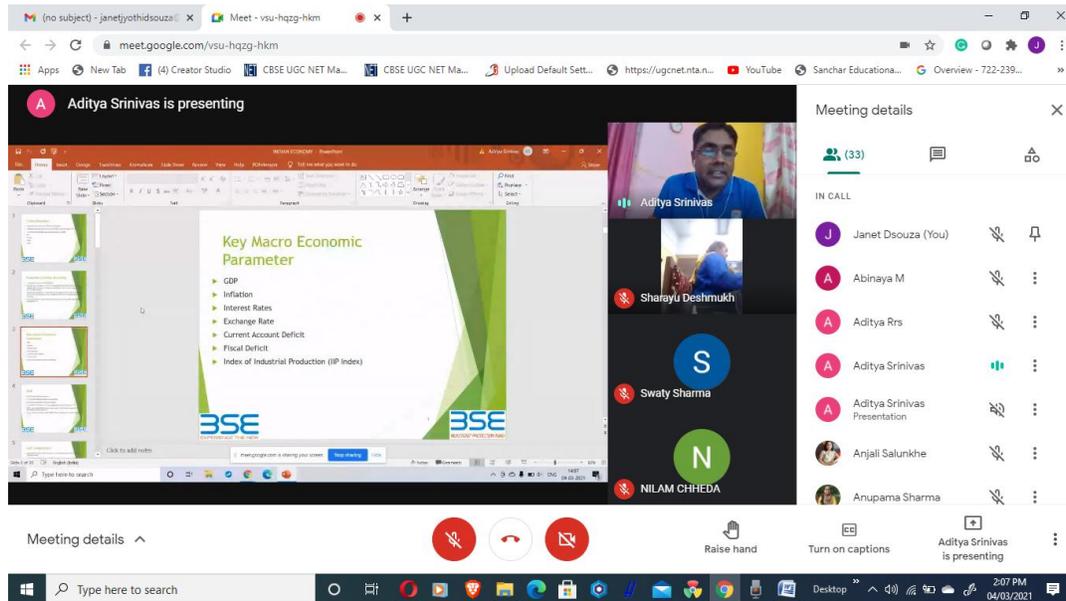
## *Outcome:*

- 1) Apply the knowledge of the investment and identify the best possible investments.
- 2) Evaluate the various investment alternatives and make investment decisions

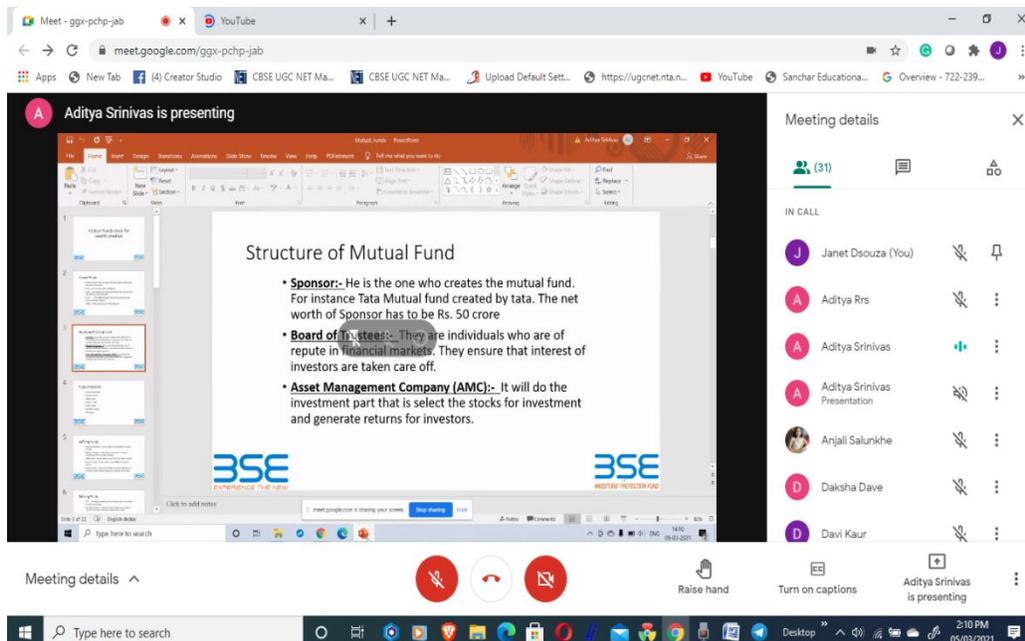
# PHOTOS

## 3 day FDP: Investing with Confidence during Pandemic, Date: 04/03/2021-06/03/2021

### Day-1



### Day 2



## Day-3

Meeting details

(27)

IN CALL

- Janet Dsouza (You)
- Aditya Rrs
- Aditya Srinivas
- Anjali Salunkhe
- br spandana
- Chandrasekar Chandru
- CHITRANSHU GARG

Meeting details

Raise hand Turn on captions Present now

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## Day -4

Meeting details

(27)

IN CALL

- Janet Dsouza (You)
- Aditya Rrs
- Aditya Srinivas
- Anjali Salunkhe
- br spandana
- Chandrasekar Chandru
- CHITRANSHU GARG

Meeting details

Aditya Srinivas  
FEB 2021 GST 1.13 LAKH CRORE

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### 3 day FDP: Investing with Confidence during Pandemic

**Resource Person: Dr.V.Aditya Srinivas Chief Operating Officer & Chief Economist Bombay Stock Exchange Broker**

**Event Co-Ordinators: Dr Janet Jyothi D'Souza & Dinesh K Date 04/03/2021-06/03/2021**

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“FDP-PORTFOLIO MANAGEMENT”

## CERTIFICATION OF PARTICIPATION

This is to certify that

Mr./Ms **DINESH K**

From **Ballari Institute of Technology and Management**

has attended a course on the

“Faculty Development Program-Portfolio Management by Bombay Stock Exchange Broker’s Forum.” The course was Organized by **Ballari Institute of Technology Management Ballari Karnataka** In collaboration with Bombay Stock Exchange.

*V. Aditya*

Dr.V.Aditya Srinivas

Chief Operating Officer & Chief Economist

BSE Broker forums



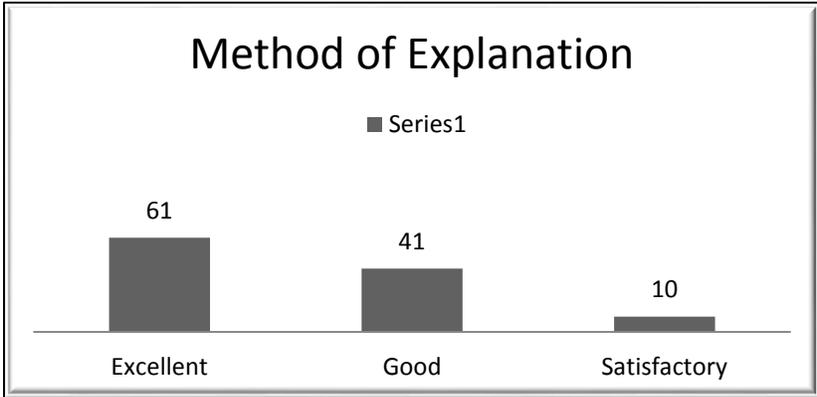
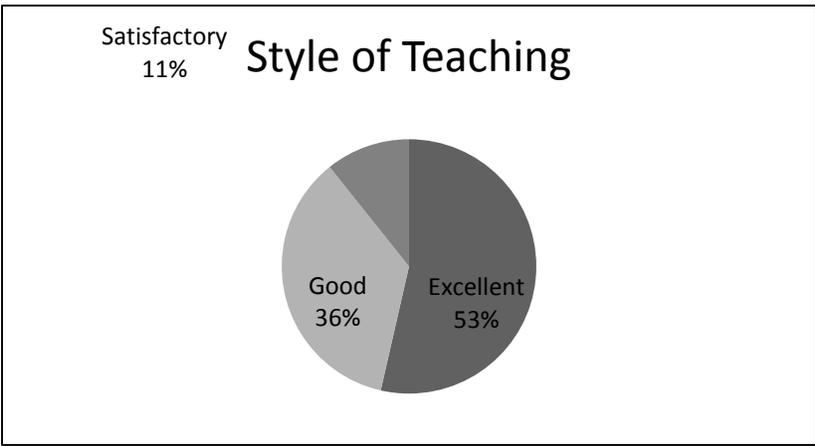
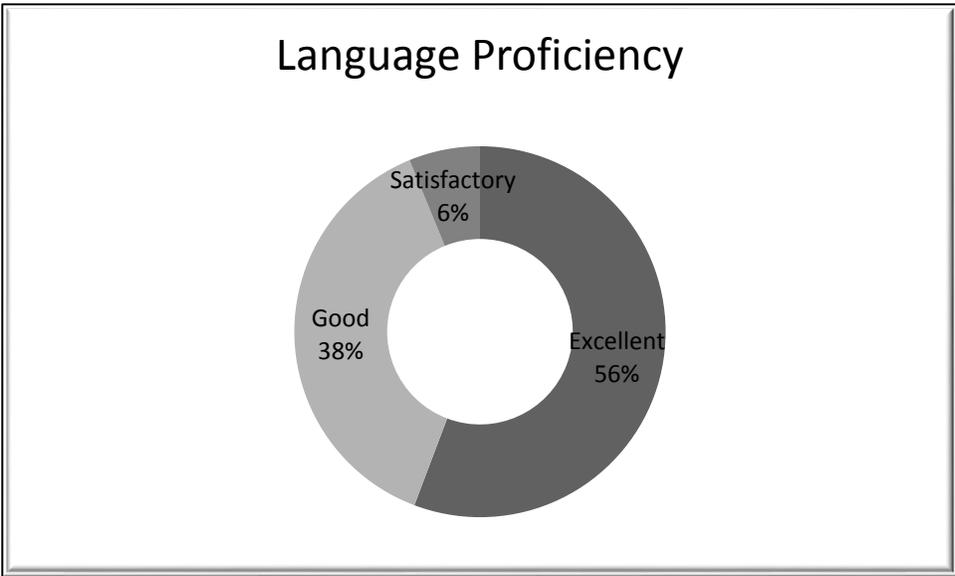
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# Feedback report

3 day FDP: Investing with Confidence during Pandemic

Resource Person: Dr.V.Aditya Srinivas Chief Operating Officer & Chief Economist Bombay Stock Exchange Broker  
Event Co-Ordinators Dr Janet Jyothi D'Souza & Dinesh K **Date** of event: 04/03/2021-06/03/2021



Basavarajeswari Group of Institutions

# BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT, BALLARI, KARNATAKA

In Collaboration with VTU & ISTE

Organized by Department of Library & Information Centre



One day Online  
Faculty Development Program  
on

## “e-Resources in Teaching, Learning and Research”

On Friday, 12<sup>th</sup> March 2021  
Timings: 10:00 am to 1.00 pm

### Aims and Objectives of the FDP:-

The programme is aimed at awareness on technical platforms like;

- > Knimbus
- > Turnitin (plagiarism check Tool)
- > NetAnalytiks Sententia (Writing Grammar Tool)

### Major Topics:

- > Effective utilization of e-resources using Knimbus Digital Library
- > User Awareness Program on Turnitin
- > Usefulness of NetAnalytiks Grammar Tool in Report Writing.

**knimbus**

Your library. Anywhere. Any device.

**NET  
ANALYTIKS**

**sententia**

**turnitin**

**turnitin**

### RESOURCE PERSONS

#### Mr. Venkatesh V

Senior Consultant, Knimbus  
Topic: Effective utilization of e-resources  
using Knimbus Digital Library  
Timings: 10:00 am to 11:00 am

#### Mr. Akshay Prasanna

Senior Consultant, PES - South Asia  
Topic: User Awareness Program on Turnitin  
Timings: 11:00 am to 12:15 pm

#### Mr. Sateesh Hegde

Head of Growth,  
NetAnalytiks Tech. Pvt. Ltd., B'lore  
Topic: Usefulness of NetAnalytiks  
Grammar Tool in Report Writing.  
Timings: 12:15 pm to 01:00 pm

### Who can Participate?

Academicians, Faculty members,  
Research Scholars, Students and  
LIS members of VTU affiliated Institutions.

**Registration:** No Registration Fee.  
Last Date of Registration: 10/03/2021

Kindly confirm the registration through  
the link:

<https://forms.gle/WhunhSr4sqm4FhFE6>



### More Details Contact:

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Basavarajeswari Group of Institutions

# BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT



(A Unit of T.E.H.R.D. Trust ©) NBA\* & NAAC Accredited & ISO 9001:2015 Certified Institution  
(Recognized by Govt. of Karnataka, Approved by AICTE, New Delhi & Affiliated to VTU, Belagavi)



**"Jnana Gangotri" Campus, #873/2, Ballari-Hosapete Road, Near Allipura,  
Ballari - 583 104 (Karnataka) [www.bitm.edu.in](http://www.bitm.edu.in)**



Ballari Institute of Technology & Management (BITM), Ballari was started under the aegis of Tungabhadra Education Health & Rural Development Trust(R), Ballari in the year 1997, with the aim of providing quality education.

BITM is one of the well-established premier Engineering & Management Colleges with the objective of imparting technical education, management education, research and training to meet the challenges of 21st Century. It empowers the Students with technical & managerial skills, professional ethics & values, and an appreciation of human creativity & innovation for an Inclusive mind.



BITM has many benchmarking activities to its credit. It is accredited with National Board of Accreditation (NBA) and National Assessment & Accreditation Council (NAAC), Recognized by Government of Karnataka, Approved by All India Council of Technical Education (AICTE), New Delhi and affiliated to Visvesvaraya Technological University, Belagavi, It has also got ISO 9001:2015 Certification.

It offers BE in CSE, ECE, EEE, ME, Civil, AI&ML and MBA. It has also been recognized as Research Centre under VTU in CSE, ECE, ME, EEE, MBA, Physics, Chemistry and Maths.

#### About BITM Knowledge Centre:

BITM Library is also known as Knowledge Centre, is an Integral part of the Institution and also the life line of academic activities. The library stretches over an area of 1100.96 Sq.Mts. with a seating capacity of about 500 members. Library has collection of 98,897 volumes of Books with 10,821 titles on Engineering, Management and Humanities. Library subscribes to 48 print copies of journals [National & International] online e-resource packages subscribed through VTU Consortium [1661 e-Journals and 11,111 e-Books (Taylor & Francis, Packt, McGraw-Hill, Elsevier, & New Age International). Digital library upgraded with 05 Terabyte data of VTU & Video Lectures and PDF from VTU E-learning, Mysuru. Library is member of VTU - Consortium and National Digital Library of India (NIL). Library has Security systems with closed Circuit Television System (CCTV).



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Chairman & Director, BITM, Ballari.

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#### COORDINATOR

**Mr. S Jaffer Basha**  
Chief Librarian

#### CONVENER

**Prof. A. Venkateshwar**  
Asst. Prof. Dept. of CSE, BITM

# WORKSHOP REPORT

One day workshop on “**E-Resources in Teaching, Learning and Research**” has been organized by the Department of Library for the faculty members. The program was jointly coordinated by VTU-Consortium, Belagavi. The objective of the workshop was to offer details on various features of technological tools like Knimbus, Turnitin, & Net Analytikis subscribed through VTU-Consortium. The program details are as follows:

1. Name of the event : “E-Resources in Teaching, Learning and Research”
2. Date : 12-03-2021
3. Time : 10AM To 1:00 PM
4. Venue : Online platform-Google meet
- Resource Persons :
  - 1) Mr. Venkatesh, V.,  
Senior Consultant, Knimbus
  - 2) Mr. Akshay Prasanna,  
Senior Consultant,  
PES South Asia, Turnitin
  - 3) Mr. Sateesh Hegde,  
Head of Growth, NetAnalytikis  
Technologies Pvt Ltd, Blore
5. Workshop Co-ordinator : Prof. Venkateshwar, A (Asst. Prof: Computer Science Dept.)

## Objectives of the Workshop:

- To bring awareness about the importance of the e-resources subscribed by the Institution.
- Knimbus remote access utilization using mLibrary mobile app.
- To bring awareness about Net Analytikis Grammar Tool in Report writing.
- To bring awareness about the features of Turnitin plagiarism check tool.

## Outcome:

- Importance of e-resources and technical tools in innovation in the current era as it clearly has an impact on the academics delivered to the participants. Since it is very useful and becoming more popular, technical tools is a good solution to create an active platform for learning.
- The usage of various parameters and methods to check plagiarism were discussed.
- All participants appreciated the usefulness of Net Analytikis grammer tool in writing.



Basavarajeswari Group of Institutions  
**BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT**

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## KNOWLEDGE CENTRE

Knowledge Centre is organizing One day FDP  
On

“E-Resources in Teaching, Learning and Research”

Dated: 12th March 2021

### SCHEDULE



TIME	Event	RESOURCE	Topic
● 10:00 Am to 11:00 Am	<b>Knimbus</b> knimbus	<b>Mr. Venkatesh V</b> venkatesh@knimbus.com 8722937551.	Effective utilization of e-resources using knimbus digital library
11:00 AM to 12:15 PM	<b>Turnitin</b> (plagiarism check Tool) turnitin	<b>Mr. Akshay Prasanna</b> Senior Consultant PES - South Asia +91 - 7290021529 Mobile - +91 - 7290021529 Email: aprasanna@turnitin.com	User Awareness Program @ BITM - Bellary
12:15 PM To ● 1:00 PM	<b>NetAnalytiks</b> Sententia (Writing Grammar Tool) NET ANALYTIKS sententia	<b>Mr. Sateesh Hegde</b> Head of Growth, NetAnalytiks Technologies Pvt Ltd Bangalore 9448091428   7022391425   sateeshh@netanalytiks.com	Usefulness of NetAnalytiks Grammar tool in report writing.

Library Coordinator

Co-Ordinator

Dept. of Library

Ballari Institute of Technology & Management  
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184	Dr.Satish S.Uplaonkar	s.uplaonkar@gmail.com	Visvesvaraya Technological University ,Centre for PG Studies ,Kalaburagi	M.B.A
185	Mr G Jaganesh Chengappa	jaganesh@yit.edu.in	Yenepoya institute of technology, Mangalore	ME



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## **BALLARI INSTITUTE OF TECHNOLOGY AND MANAGEMENT**

(A Unit of T.E.H.R.D Trust ©) NBA\* & NAAC Accredited & ISO 9001:2015 Certified Institute.,  
"Jnana Gangotri" Campus, #873/2, Ballari-Hosapete Road, Near Allipur, Ballari - 583104,  
Karnataka)



### CERTIFICATE OF PARTICIPATION

**Mr. S.JAFFER BASHA** of **BALLARI INSTITUTE OF TECHNOLOGY AND MANAGEMENT, BALLARI** has participated in One day online FDP on **"e-Resources in Teaching, Learning and Research"** conducted on March 12<sup>th</sup>, 2021. Organized by Department of Library and Information Centre in Collaboration with VTU and ISTE.

**Prof. A. Venkateshwar**  
Convener

**Dr. V.C. Patil**  
Principal, BITM

**BALLARI INSTITUTE OF TECHNOLOGY AND MANAGEMENT, BALLARI**  
**Participation Confirmation for the One day FDP on**  
**“E-Resources in Teaching, Learning and Research”**

12<sup>th</sup> March 2021

Dear All,

Greetings from Ballari Institute of Technology and Management, Ballari!!!!  
Welcome to the one-day online FDP on “E-Resources in Teaching, Learning and Research” dated  
12<sup>th</sup> March 2021.

Please find the **Links** to join the FDP.

**Session-1 Microsoft Teams Platform [Timing: 10:00 am to 11:00 am]**

[https://teams.microsoft.com/l/meetup-join/19%3ameeting\\_M2Y1ZDBmNjEtZjlkZC00YmZkLWE4ODYtOWVjYjYzMDJjMWJi%40thread.v2/0?context=%7b%22Tid%22%3a%22c92b265c-b363-4cec-9086-9faed40415a9%22%2c%22Oid%22%3a%2225bda281-2f10-4918-808b-9a848e8248a1%22%7d](https://teams.microsoft.com/l/meetup-join/19%3ameeting_M2Y1ZDBmNjEtZjlkZC00YmZkLWE4ODYtOWVjYjYzMDJjMWJi%40thread.v2/0?context=%7b%22Tid%22%3a%22c92b265c-b363-4cec-9086-9faed40415a9%22%2c%22Oid%22%3a%2225bda281-2f10-4918-808b-9a848e8248a1%22%7d)

**Session-2 Zoom Platform [Timing 11:00 am to 12:15 pm]**

<https://turnitin.zoom.us/join/register/tJcvcOGsqTwpHNxomhrQ1BHNgENe4fcLfCtr>

**\*\*Note:** Register in advance for this meeting using the above link, after registering you will receive a confirmation email containing information about joining the meeting.

**Session-3 Google Meet Platform [Timing 12:15 pm to 1:00 pm]**

<https://meet.google.com/rji-aznh-upt>

**Below are the instructions for the participants**

Participants are requested to install **Microsoft teams, Zoom and Google meet** apps in advance as the three different speakers are using their own platform.

Participants are requested to join **10 minutes prior** to the commencement of the session.

All the participants should keep their **cameras off** and **mute** their **audio** throughout the sessions.

If you have any queries regarding the talk during the session, we request you to wait till the session gets over. Share your queries through **chat-box**.

*Participants will be provided with the e-certificate only after giving feedback, the link of which will be mailed immediately after the last session.*

For Any Queries Contact

Mr. Dadapeer	8867513685
Mr. Usman K	9538492636
Mr. Manjunath G	9164658445



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**VISVESVARAYA TECHNOLOGICAL UNIVERSITY**  
**BALLARI INSTITUTE OF TECHNOLOGY &  
 MANAGEMENT**

"Jnana Gangotri" Campus, #873/2, Ballari-Hosapete Road, Allipura, Ballari,  
 Karnataka.

**5 Days FDP on Internet of**

**Intelligent of Things  
 & Machine Learning.**

**Date :**  
 10 - 14th Nov, 2020

**Time :**  
 11:00 AM - 2:00 PM

**Patron:**



**Dr. Yashvant Bhupal**  
 Director, BITM.



**Prof. Prithviraj Y J**  
 Deputy Director, BITM.



**Mr. Puneet Kumar Mishra**  
 Chair, IEEE Bangalore Section



**Dr. Parmeshachari B D**  
 Prof. & Head Department of TCE  
 GSSSIET, Mysuru.

**Chief Guest:**



**Dr. Sanju Tiwari** Senior Researcher,  
 Universidad Automata de Tamaulipas, Mexico.  
**Topic:** Representing Knowledge in Web of Data:  
 A Vision of Semantic Web.  
**Date:** 10th Nov, 11:00 AM

**Key Note:**



**Dr. Rashmi Agarwal** Professor,  
 Manav Rachna International Institute of Research & Studies  
 Faridabad, India.  
**Topic:** Research in Big Data & Machine Learning.  
**Date:** 11th Nov, 11:00 AM



**Celestine Iwendi** Senior Member of IEEE,  
 Fellow of Higher Education Academy, United  
 Kingdom.  
**Topic:** Securing The Internet of Intelligent of Things  
 (INTRUXIT)  
**Date:** 12th Nov, 1:30 PM

**Convener:**

**Dr. U. Eranna** Prof. & HOD Department of ECE, BITM.  
**Dr. Sadyojatha K M** Prof. Department of ECE, BITM.

**IEEE Branch Counsellor:**

**Dr. Abdul Lateef Haroon P S**  
 Department of ECE, BITM

**Further Details Contact:**

Dr. Abdul Lateef Haroon P S  
 IEEE Branch Counsellor  
 Ph no: +91 - 9738973034

**Registration Link:**

<https://qr.go.page.link/zjXqV>

E - Certificates will be provided to all the Participants.

**Guest of Honour:**

**Dr. V C Patil** Principal, BITM.  
**Dr. Yadavalli Basavaraj** Vice - Principal, BITM.

**Organizing Committee:**

**Dr. Abdul Lateef Haroon P S**  
 Department of ECE, BITM.  
**Mr. Premachand D R**  
 Department of ECE, BITM.  
 All the faculties, Department of ECE, BITM.  
 All the Students, IEEE SB, BITM.

**Meeting  
 Id:**

It will be shared on the previous day of the session  
 to your respective mail id .

SCAN TO REGISTER



## WORKSHOP REPORT

Five day online FDP on “**5 Days Faculty Development Program on Internet of Intelligent of Things & Machine Learning**” has been organised by the Department of Electronics and Communication Engineering for the faculty members. The objective of the workshop was to offer detailed hands on experience on various aspects of VLSI design using Cadence tools.

The program details are as follows:

1. Name of the event : **5 Days Faculty Development Program on Internet of Intelligent of Things & Machine Learning**
2. Dates : 10-11-2022 to 14-11-2020
3. Time : 10AM To 4:30 PM
4. Venue : EC Seminar Hall
5. Resource Persons : Dr. Sanju Tiwari  
Dr. Celestine Iwendi  
Dr. Rashmi Agarwal
6. Workshop Co-ordinator : Dr. Abdul Lateef Haroon P S

### Objectives of the Workshop:

- To provide an industry-academia platform
- To enhance the vision of semantic web
- To realize the various types of Ransomware Attacks in IoT.

### Outcome:

- Participants understood and given industry-academia platform.
- Participants have understood the clear view of semantic web
- Participants carried out various case studies to realize Ransomware Attacks in IoT.

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Searching: Lokesh K.S. K.S.

Participants (51)

Panelist: 32

Dr. Abdul...	Roshni Agrawal	Manjunath K M RVT...	Renuka Bai	
S.Hetu Jayad	Sarika G	venkateshwar a	ajina R VITM	Chalka Srinitha
Dishadbanu J	Dr. PARAMESHCHARI	Gurusai Biradar	K N SREENIVAS RAO	Lokesh K.S. K.S.
Kasamsetty Keerthi	LAKSHMI RAJ...	Manjunath G	Manjunath HR	Nilam Chheda
Premachand D R	Raymond Inadaryaj	Sadyojatha k m	SAGARA T V	Sahana P M

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Participants (55)

Panelist: 50

Dr. Abdul...	x.hanshitha	Webex MGA-WebEx...	Dr. PARAMESHCH...	ASHA SHANKARATHOTA
Dr. Sanju Tiwari	shikhar K M	Abhisha Patel	Aishwarya p kiravadi	ajina a
AKHILA K	Ambayya	Archana	Basava Rajeshwari	Dadaper p
DAVINI BHARATH REDDY	Deepak Sharma K M	Dishadbanu	Dr. Nooralath Shariff C	Dr.U.Eranna
Gurusai	HEMANTHUMMAR KAPP	JAYALKAR VINAY	K N SREENIVAS RAO	K.Keerthi

Chat

FROM: ASHILA KAZEE MARULAN P 2 (2) WEBEX MGA-WebEx India Council (private): 11:20 AM  
 can u hear us sir  
 from MANJUNATH KM RITHM BENGALURU (private): 11:20 AM  
 pls check with voice abdul sir

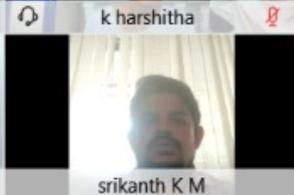
To: Webex MGA-WebEx-India-Council

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Q&A

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88 🗨️

 Dr. ABDUL L... (Host...)	 k harshitha	 Webex MGA-WebEx...	 Dr. PARAMESHACH...	 ASHA SHANKARATHOTA
 Dr. Sanju Tiwari	 srikanth K M	Abhilasha Patil	Aishwarya p kiruvadi	ajina a
AKHILA K	Ambrayya	Archana	Basava Rajeshwari	Dadapeer p
DAVINTI BHARATH REDDY	Deepak Sharma K M	Dilshadbanu	Dr. Noorullah Shariff C	Dr.U.Eranna
Gurusai	HEMANTHAKUMAR KAPP	JAVALKAR VINAY	K N SREENIVAS RAO	K. Keerthi

Participants (55) ✕

🔍 Search

Panelist: 50

-   Dr. ABDUL ...  
Host, me  
-  venkateshwar a
-  ASHA SHANKARATHOTA 
-  MANASA K CHIG... 

Chat ✕

FROM DR. ABDUL LAIEEF HAROON P S TO Webex MGA-WebEx-India-Council (privately): 11:20 AM  
can u hear us sir

from MANJUNATH KM RVITM BENGALURU (privately): 11:28 AM  
pls check with voice abdul sir

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Q&A ✕

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Speaking: Dr. PARAMESHACHARI B D



K N SREENIVAS RAO	K. Keerthi 📺 🔊	keerthana	M. Shruthi 📺 🔊	Manjunatha S
Mohammed Shafiulla	Prathiba Shanbog	premachand D R	Raymond Irudayaraj 📺 🔊	Renuka v tali 📺 🔊
Rohit Patil	saddukm 📺 🔊	Sadyojatha k m 🔊 🔊	Sagara T V 📺 🔊	SAHANA 📺 🔊
sathya.smg 📺 🔊	Savitha G	Shilpa K R 📺 🔊	Shivnarayan Vaidyanathan	simantini Roy roychowdh
sishitha chakka 📺 🔊	sowbhagya.B 📺 🔊	srikanth K M	Swetha N	Ulaganathan Jayapal 📺 🔊

Participants (54) ✕

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Panelist: 46

- DS 🔄 Dr. ABDUL ...  
Host, me 🔊 🔊
- AS 🔄 ASHA SHANKARATHOTA 🔊 🔊
- MB MANJUNATH KM RVITM BENG... 🔊
- AP Abhilasha Patil

Chat ✕

India-Council (privately): 11:20 AM  
**good morning sir**  
 from Dr. ABDUL LATEEF HAROON P S to Webex MGA-WebEx-India-Council (privately): 11:20 AM  
**can u hear us sir**  
 from MANJUNATH KM RVITM BENGALURU (privately): 11:28 AM

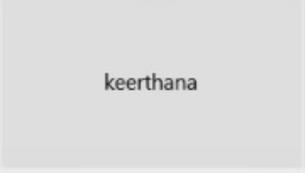
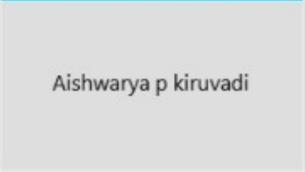
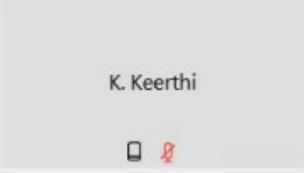
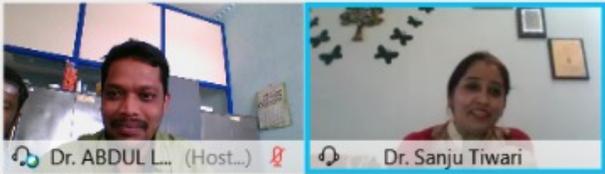
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> Q&A ✕

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Speaking: Dr. Sanju Tiwari, Dr. PARAMESHACHARI B D



**Participants (54)**

Search

**Panelist: 46**

- DS Dr. ABDUL ... Host, me
- AS ASHA SHANKARATHOTA
- MB MANJUNATH KM RVITM BENG...

**Chat**

India-Council (privately): 11:20 AM  
good morning sir  
from Dr. ABDUL LATEEF HAROON P S to Webex MGA-WebEx-India-Council (privately): 11:20 AM  
can u hear us sir  
from MANJUNATH KM RVITM BENGALURU (privately): 11:28 AM  
pls check with voice abdul sir

To: Everyone

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**Q&A**

Speaking: Dr. PARAMESHACHARI B D

88

Dr. ABDUL LATEEF HARO... Host, me 	k harshitha 	 Dr. PARAMESHACH...	Dr.U.Eranna 	 ASHA SHANKARAT...
 MANJUNATH KM RVITM BEN...	Abhilasha Patil	Aishwarya p kiruvadi	ajina a	AKHILA K
< Archana	Basava Rajeshwari 	Dadapeer p 	DAVINTI BHARATH REDDY	Deepak Sharma K >
Dilshadbanu 	Dr. Noorullah Shariff C	Dr. Sanju Tiwari 	Gurusai 	HEMANTHAKUMAR KAPP 
JAVALKAR VINAY	K N SREENIVAS RAO	K. Keerthi 	keerthana	M. Shruthi 

**Participants (54)**

Search

**Panelist: 46**

- DS Dr. ABDUL ...  
Host, me
- AS ASHA SHANKARATHOTA
- MB MANJUNATH KM RVITM BENG...
- AP Abhilasha Patil

**Chat**

India-Council (privately): 11:20 AM  
good morning sir  
from Dr. ABDUL LATEEF HAROON P S to Webex MGA-WebEx-India-Council (privately): 11:20 AM  
can u hear us sir  
from MANJUNATH KM RVITM BENGALURU (privately): 11:28 AM

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**Q&A**

Participant list: Dr. ABDUL LATEEF HAR... (Host, me), **Dr. Sanju Tiwari**, premachand D R, Dr. PARAMESHACHARI, Raymond Irudayaraj, saddukm

# Outline

- Data, Information, Knowledge
- Representing Knowledge
- Knowledge in Linguistics
- Knowledge Representation For...
- Knowledge Representation La...
- Web of Data
- Evolution of WWW
- WWW and Semantic Web
- Ontology, Ontology Tools
- Demo of Tools

### Attendee List

Search:  Find

Select all

Name (41)	Feedback
Manjunatha S	
Poojitha	
PRABHAKAR K	
Prathiba Shanbog	
Renuka v tali	
Rohit Patil	
Sagara T V	

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### Participants (49)

Attendee: 41 (2 displayed)

- MB MANJUNAT...
- AA ajina a

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### Chat

where is video option  
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whether i am visible  
from Dr. PARAMESHACHARI B D to host (privately): 11:16 AM  
Fine thank you  
from Dr. ABDUL LATEEF HAROON P S to Webex MGA-WebEx-India-Council (privately): 11:20 AM  
good morning sir  
from Dr. ABDUL LATEEF HAROON P S to Webex MGA-WebEx-India-Council (privately): 11:20 AM  
can u hear us sir  
from MANJUNATH KM RVITM BENGALURU (privately): 11:28 AM

To: Everyone

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> Q&A

Participant bar showing: Dr. ABDUL LATEEF HAR... (Host, me), Dr. Sanju Tiwari (video on), premachand D R, Raymond Irudayaraj, Sadyojatha k m, Ulaganathan Jayapal.

Viewing Dr. Sanju Tiwari's ap...

# Semantic Web (Architecture)

## Set of Resources:

Professor(Oscar Corcho)  
 PhDStudent(David, Paola, Shaurya)

## Properties:

isSupervisorOf(Oscar, David)  
 isSupervisorOf(Oscar, Paola)

## OWL: Ontologies and Reasoning

Powerful formalism to represent classes of object and their properties in form of ontologies

Sharing of ontologies

Logical inferences over data

Defining rules over data

Powerful reasoning framework, Description Logics

### Participants (46)

Search

#### Panelist: 6

- DS Dr. ABDUL L... (Host, me)
- DT Dr. Sanju Tiwari
- PR premachand D R
- RI Raymond Irudayaraj
- SM Sadyojatha k m
- UJ Ulaganathan Jayapal

#### Attendee: 40 (1 displayed)

- AA ajina a ?

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> Q&A

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Participants | Chat

Participant list: Dr. ABDUL LATEEF HAR... (Host, me), **Dr. Sanju Tiwari**, Dr.U.Eranna, Dr. PARAMESHACHARI, premachand D R, Raymond Irudayaraj

Participants (53)

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- MB MANJUNAT...

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whether i am visible  
from Dr. PARAMESHACHARI B D to host (privately): 11:16 AM  
Fine thank you  
from Dr. ABDUL LATEEF HAROON P S to Webex MGA-WebEx-India-Council (privately): 11:20 AM  
good morning sir  
from Dr. ABDUL LATEEF HAROON P S to Webex MGA-WebEx-India-Council (privately): 11:20 AM  
can u hear us sir  
from MANJUNATH KM RVITM BENGALURU (privately): 11:26 AM

pls check with voice abdul sir

To: Everyone

Enter chat message here

> Q&A

Webinar Series-2020  
BITM, Ballari, Karnataka



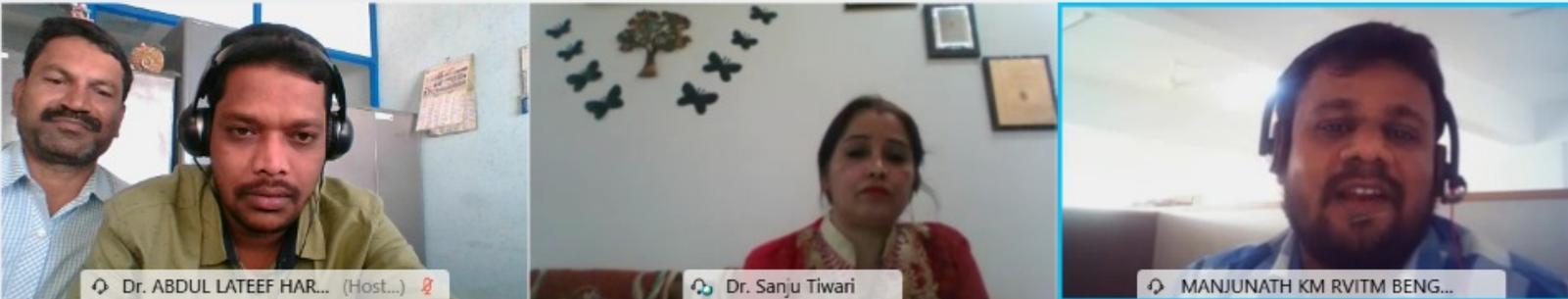
Representing Knowledge in Web of Data: A Vision of Semantic Web

Dr. Sanju Tiwari, (PhD, Post-Doc)  
Universidad Autonoma de Tamaulipas, Mexico  
twarisanju18@ieee.org

Click to add notes

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Speaking: MANJUNATH KM RVITM BENGALURU



Deepak Sharma K M

premachand D R

Raymond Irudayaraj

Sadyojatha k m

Ulaganathan Jayapal

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**5 Days FDP on Internet of  
Intelligent of Things  
& Machine Learning.**

**Resource Person: Dr. Sanju Tiwari, Dr. Celestine Iwendi, Dr. Rashmi Agarwal  
Event Co-Ordinator: Dr Abdul Lateef Haroon P S 10/11/2020-14/11/2020**

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# BALLARI INSTITUTE OF TECHNOLOGY AND MANAGEMENT

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## CERTIFICATE OF PARTICIPATION

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in appreciation for participation in the Webinar on " 5 Days FACULTY DEVELOPMENT PROGRAM on INTERNET OF INTELLIGENT THINGS & MACHINE LEARNING" organized by BITM IEEE Student Branch in association with IEEE Bangalore Section and CAS Bangalore chapter held from 10-14th November, 2020.

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**Agenda:**

- Introduction
- What are plagiarism and its effect on an Institution?
- Why Turnitin Originality Check
- Instructor Management/ Student Management
- Creation of class and Assignment.
- Student Paper submission and review.
- Generation of Similarity Reports in Turnitin.
- Similarity Report download.
- Q& A

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# Online - Faculty User Awareness Program VTU – Consortium – Cluster 2 North Karnataka



## Agenda :

- Introduction
- What are plagiarism and its effect ?
- Why Turnitin Originality Check
- Student Management
- Creation of class and Assignment.
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Senior PES – Specialist  
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If any one want to ask a question, please unmute your mike and ask question, or put your question through chat it self.
- KSGI 42:04  
Could u load one paper as an example?

Search the web and Windows | Address | 10:08 AM 1/4/2022

# WORKSHOP REPORT

One day workshop on “**Online-Faculty User Awareness Program VTU-Consortium-Cluster 2 North Karnataka**” has been organized by the Department of Library for the faculty members. The program was jointly coordinated by VTU-Consortium, Belagavi. The objective of the workshop was to offer detailed on various features of plagiarisms check tool “turnitin” subscribed through VTU-Consortium.

The program details are as follows:

1. Name of the event : Online-Faculty User Awareness Program VTU-Consortium-Cluster 2 North Karnataka”
2. Date : 04-12-2020
3. Time : 10:30 AM
4. Venue : Online
5. Resource Persons : Mr. Akshay Prasanna,  
Senior PES Specialist,  
PES South Asia, Turnitin

Workshop Co-ordinator : Prof. Venkateshwar, A (Asst. Prof: Computer Science Dept.)

## **Objectives of the Workshop:**

- Create awareness about plagiarism in research
- To avoid plagiarism in order to write with integrity.
- Generation of similarity reports in turnitin by admin and instructor.

## **Outcome:**

- Participants familiarized plagiarism which means using someone else’s work without giving them proper credit.
- Participants learnt the procedure and methods to check plagiarism.
- The turnitin prevents duplication of research work and even the slightly changed or variation in research.



**BALLARI INSTITUTE OF TECHNOLOGY AND MANAGEMENT, BALLARI**

Organized by: Department of Mechanical Engineering

In association with BITM - IQAC



**Live webinar Series - Faculty Development Program**

on

**" A Paradigm Shift in Management "**

**October 5th to 9th 2020**



**Dr. Shiva Prasad C G**  
Senior Faculty, HAL Management Academy, HAL,  
Bengaluru  
Topic: "A Paradigm shift in Quality Management"  
Schedule: 05-10-2020 (2:00 - 3:00 PM)



**Dr. Savitha M**  
Associate Professor, Department of IP&E  
SJCE Musuru  
Topic: "Management Information System"  
Schedule: 08-10-2020 (11:00 AM - 12:00 PM)



**Dr. Gurram Prasad Dinesh**  
Professor, Dept. Of Management Studies,  
VSK University, Ballari  
Topic: Paradigm shift - "Building a new talent  
Management model to boost growth"  
Schedule: 06-10-2020 (2:00 - 3:00 PM)



**Dr. S Jayanna**  
Professor, Dept. Of Management studies,  
BITM, Ballari  
Topic: "Re-Engineering Classroom Practices"  
Schedule: 08-10-2020 (2:00 - 3:00 PM)



**Dr. T. Manjunatha**  
Associate Professor, Department of Mechanical Engineering  
SJCE, Mysuru  
Topic: "Hypothesis testing by statistical tools using SPSS"  
Schedule: 07-10-2020 (11:00 AM - 12:00 PM)



**Dr. Y Vijay Kumar**  
Principal, GMIT, Davangere  
Topic: "Latest Trends in Management"  
Schedule: 09-10-2020 (11:00 AM -12:00 PM)



**Dr. S Ezhil Vannan**  
Professor, Department of Mechanical Engineering  
Malnad College of Engineering, Hassan  
Topic: "Research Methodology"  
Schedule: 07-10-2020 (2:00 - 3:00 PM)

Registration Link : <https://forms.gle/F9WKxdQE1aQzD6PQ9>  
For any Queries contact:

Shivaramakrishna A [9916252513](tel:9916252513)  
Venkatesh K C [8880454511](tel:8880454511)  
Vijay Kumar B P [8494849410](tel:8494849410)  
Rajashekar K [9886848435](tel:9886848435)



**Conveners:**

**Dr. Raghavendra Joshi & Dr. V Venkata Ramana**

## **FDP REPORT**

Five day FDP on “A Paradigm Shift in Management” has been organized by the Department of Mechanical Engineering for the faculty members. The objective of the faculty development program (FDP) was to offer detailed trends on various aspects of Management concepts, switch over to the latest practices in various fields like Re – Engineering and Information systems along with applicability of statistical tools towards the research. The program details are as follows:

Name of the event : A Paradigm Shift in Management  
Date : 05-10-2020 to 09-10-2020  
Time : 9AM to 4 PM  
Venue : ON LINE  
Resource Persons : Dr. S Jayanna / Dr. G P Dinesh / Dr. Shiva Prasad /  
Dr. T. Manjunatha / Dr. Ezhil Vannan / Dr. Savitha /  
Dr. Y. Vijay Kumar  
FDP Co-ordinator : Dr. V. Venkata Ramana & Dr. Raghavendra Joshi

### **Objectives of the Workshop:**

- To create awareness on the latest trends in Management.
- To give exposure on Re- Engineering classroom practices.
- To enlighten upon building new talent management model to boost growth.
- To create awareness on Quality Management and MIS.
- To impart the knowledge on Research methodology and statistical tools.

### **Outcome:**

- Awareness about latest trends in management was created among the participants.
- The faculty gained knowledge about the Re- Engineering classroom practices.
- The participants have learnt how to apply new talent management models.
- The faculty gained the knowledge about quality management and information systems.
- The attendees learnt about the statistical tools applicability in research.



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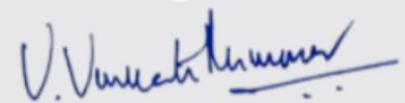
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<b>Sl No.</b>	<b>Name of the participant</b>	<b>Name of the institution</b>	<b>Email ID</b>	<b>Timestamp</b>
1	VIJAYKUMAR B P	Ballari institute of technology and managent , Ballari	bpviji6@gmail.com	2020/10/10 1:47:43 PM GMT+5:30
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4	MANJUNATHA E	Ballari institute of technology and managent, Ballari	blackswan.oxford@gmail.com	2020/10/10 1:59:21 PM GMT+5:30
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6	Pavan Kumar B K	BITM	pk22586@gmail.com	2020/10/10 2:05:07 PM GMT+5:30
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Basavarajeswari Group of Institutions



# **BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT, BALLARI (KARNATAKA)**

**Dept. of Mechanical Engineering  
Organizes**

**One Day Webinar on**

## **Overview of “Graphene” - A Prospective Material**

**Webinar Date: 8th July 2020**

**Timings: 11.00 AM to 12.30 PM**



**Resource Person**

**Dr. Ashwin. C. Gowda**

**Assistant Professor  
VTU, Muddenahalli**

**Use GOTO MEETING Application**

**For further queries get in touch with Webinar Coordinators**

**Prof. Shiva Kumar.S.Y and Prof. Md. Fayaz K**

**9916125043 / 8147282449**

# WEBINAR REPORT

One day webinar on **Overview of "Graphene"-A Prospective Material** has been organised by the Department of Mechanical Engineering for the faculty and Students.

The objective of the webinar was to offer detailed information related to Graphene special Mechanical properties and its applications across various fields.

The program details are as follows:

1. Name of the event : **Overview of "Graphene"-A Prospective Material**
2. Date : 08-07-2020
3. Time : 11AM To 12:30 PM
4. Mode of Conduct : Online
5. Application used : GOTO MEETING
5. Resource Persons : Dr. Ashwin C Gowda, Assistant Professor, VTU, Muddenahalli
6. Workshop Co-ordinator : Mr. Shiva kumar S Y, Mr. Md. Fayaz K

## **Objectives of the Webinar:**

- To provide brief introduction to advanced materials.
- To give information on how Graphene material is different from conventional materials.
- To provide information related to Graphene material properties.
- To provide information related to various application fields of Graphene material.

## **Outcome:**

- Participants understood what are advanced materials.
- Participants have learnt about material properties of Graphene material.
- Participants have learnt about various application fields of Graphene material.



**BALLARI INSTITUTE OF TECHNOLOGY &  
MANAGEMENT, BALLARI  
DEPARTMENT OF MECHANICAL ENGINEERING**



**CERTIFICATE OF PARTICIPATION**

*This is to Certify that... **Dr. Ganesh B** ..... of  
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**Coordinators:**

**Shiva Kumar S Y  
Md. Fayaz K**

**Dr. Yadavalli Basavaraj  
Vice Principal & HOD**

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**DEPARTMENT OF MECHANICAL ENGINEERING**



**CERTIFICATE OF PARTICIPATION**

*This is to Certify that... **Mr. Ravi G** ..... of  
.. Ballari Institute of Technology and Management, Ballari.. has attended 1-day online  
webinar on “**Overview of Graphene- A Prospective Material**”, Organized  
by Department of Mechanical Engineering, Ballari Institute of Technology  
& Management, Ballari on **8<sup>th</sup> July 2020** .*

**Coordinators:**

**Shiva Kumar S Y**  
**Md. Fayaz K**

**Dr. Yadavalli Basavaraj**  
**Vice Principal & HOD**

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..Ballari Institute of Technology and Management, Ballari.. has attended 1-day online  
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.. **Ballari Institute of Technology and Management, Ballari**.. has attended 1-day online  
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.. **Ballari Institute of Technology and Management, Ballari**.. has attended 1-day online  
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..Ballari Institute of Technology and Management, Ballari.. has attended 1-day online  
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*This is to Certify that..... **Mr. Mohammed Fouzan** ..... of  
..... Resaech scholar, vtu, Belagvi ..... has attended 1-day online  
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*This is to Certify that..... **Mr. Gode Pruthviraj**..... of  
..... Hanagal sri kumareshwara Polytechnic , Ballari..... has attended 1-day online  
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*This is to Certify that..... **Mr. Naveen Bharadi Shettar**..... of  
Resaech scholar, National Institute of Technology, Karnataka, Surathkal ...has attended  
1-day online webinar on “**Overview of Graphene- A Prospective  
Material**”, Organized by Department of Mechanical Engineering, Ballari  
Institute of Technology & Management, Ballari on **8<sup>th</sup> July 2020** .*

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*This is to Certify that..... **Pramod N S** ..... of  
..... **MVJ COLLEGE OF ENGINEERING, BENGALURU** ..... has attended 1-day online  
webinar on “**Overview of Graphene- A Prospective Material**”, Organized  
by Department of Mechanical Engineering, Ballari Institute of Technology  
& Management, Ballari on **8<sup>th</sup> July 2020** .*

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**Dr. Yadavalli Basavaraj**  
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*This is to Certify that..... **Mr. Suchith K S** ..... of  
...**MVJ COLLEGE OF ENGINEERING, BENGALURU**..... has attended 1-day online  
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*This is to Certify that... **Mr. Nagaraj Basavantappa Hugar**..... of  
.. **Sanjay Gandhi Polytechnic, Ballari**..... has attended 1-day online  
webinar on “**Overview of Graphene- A Prospective Material**”, Organized  
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.. **Sanjay Gandhi Polytechnic, Ballari** ..... has attended 1-day online  
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 .. Sanjay Gandhi Polytechnic, Ballari ..... has attended 1-day online  
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